



PCB@

PCB GH53G LA-L191P LS-L031P/K852P/K853P
DAZ30A00101

LOGO@

ROYALTY HDMI W/LOGO+HDCP
RO0000003HM

X4E@

SMT EMC EG0 G1 G1R FOR EE AL191 GH53G
X4EAR4BOL01

X4EFP@

SMT EMC EG0 G1 G1R FOR EE AL191 GH53G
X4EAR4BOL21

Compal Confidential

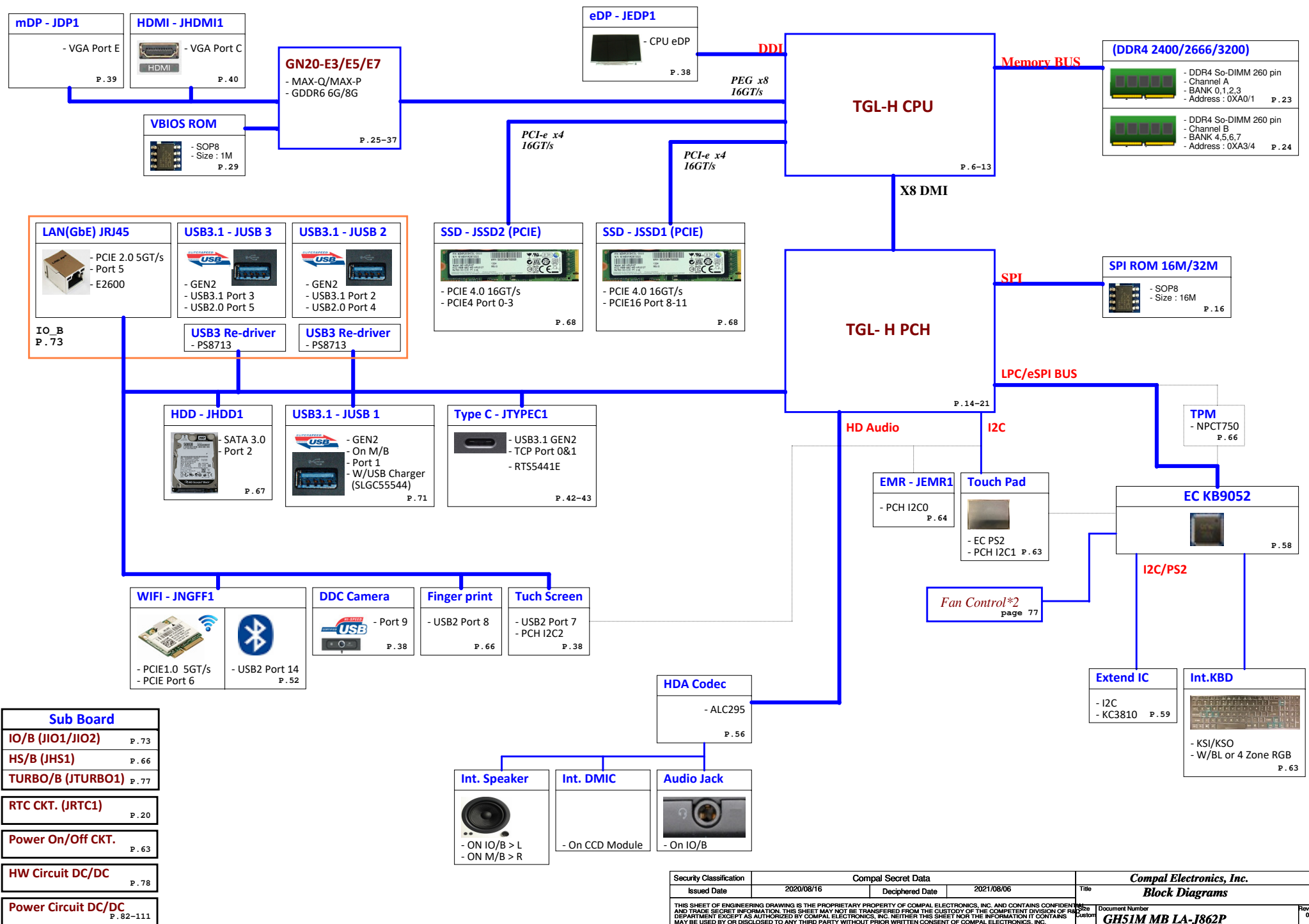
MB Schematic Document

GH51G/GH53G/GH57G/GH71G/GH73G LA-L191P

Rev:1.A

2020.04.12

Security Classification	Compal Secret Data		Title	
Issued Date	2020/08/16	Deciphered Date	2021/08/06	Compal Electronics, Inc.
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			GH51M MB LA-J862P	0.1
			Date: Monday, April 12, 2021	Sheet 1 of 112



Vcc	3.3V +/- 5%	EC Board ID Table for AD channel			
Ra	100K +/- 1%				
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
* 9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
* 13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFF
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

Board ID	PCB Revision
0	50 Rev0.1
1	50 Rev0.2
2	50 Rev1.0
3	
4	50 Rev0.1+RGB
5	50 Rev0.2+RGB
6	50 Rev1.0+RGB
7	
8	60 Rev0.1
9	60 Rev0.2/1.0/3
10	
11	
12	60 Rev0.1+RGB
13	60 Rev0.2/1.0/3
14	
15	
16	
17	
18	
19	
	*PCB Version *Key board type

```
For PreMP BOM 4/12
keep EVT2 setting
ID:9 (100K)
ID:13 (240K)
```

SIGNAL	SLP_S#3	SLP_S#4	SLP_S#5	+VALW	+V	+VS
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF

Power Plane	Description	S0	S3	S4	S5
+RTVCCT	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_1 (+3V_PRIM)	TM-P3393-003 (Touch Pad)			
I2C_5 (+3VS)	(Touch Screen)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML0CLK (+1.8VALW)	BURNSIDE-BRIDGE 1	0x53		
	BURNSIDE-BRIDGE 2	0x54		
PCH_SML1CLK (+1.8VALW)	PD PTPS65991	0x21		
	(EC)			
EC_SMB_CK0 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK1 (+3VLP_EC)	GN20 E3/E5/E7 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	Thermal Sensor (G781)	1001_1010b	1001_1010b	1001_1010b
	(PCH)			
EC_SMB_CK2 (+5VS)	LED driver	0xC0		
	(PER KEY)			

KC3810 0xC0

Item (X43)	BOM Structure	Item (X43)	BOM Structure
pop	@	eDP-TS USB	TS_USB@ V
rector	CONN@	eDP-TS I2C	TS_I2C@
	PCB@ V	USB C circuit	TypeC@ V
Only(Reserved)	UMA@	mDP	DP@ V
		For Acer IOAC	IOAC@ V
id ID	EVT@ V	No Acer IOAC	NOIAC@ V
id ID RGB	EVTRGB@	Intel CNVI	CNVI@ V
5 CPU QWCC	QWCC@ V		
7 CPU QWCB	QWCB@ V	FOR UART debug	UART@
PCH	HM570@ V	Extend GPIO	KC3810@ V
J circuit	VGA@ V	Finger Print	FP@ V
GN20_E3	E3_PS@ V	KB backlight	KBLED@ V
GN20_E5	E5_PS@ V	KB LED driver	LED14P@ V
GN20_E7	E7_PS@	CMC signal	CMC@ V
		Thermal sensor	TMS@ V
request reserve	Glitch@	TPM pop	TPM@ V
request reserve	@Glitch@		
LE5 sample issue	ES@ V	OVRM pop	OVRM@ V
		OVRM GEN1 pop	GEN1@
device	1LD@	UPI OVRM GEN1 pop	UPI_GEN1@
device	2LD@ V	OVRM GEN2 pop	GEN2@
1B Rom part	32MB@	ON OVRM GEN2 pop	ON_GEN2@
1B Rom part	16MB@ V	UPI OVRM GEN2 pop	UPI_GEN2@
		12VFAN POWER	12VFAN@
PM POWER RAIL	PREM@	5VFAN POWER	5VFAN@ V
POWER RAIL	VEL@		
KEY CIRCUIT	PERKEY@ V	HDMI ROYALTY	LOGO@

[illegible]

Item (X4E)	BOM Structure
EMI requirement	EMI@ V
EMI require reserve	XEMI@
ESD requirement	ESD@ V
ESD require reserve	XESD@
FP ESD requirement	FPESD@ V
X4EAR3BOL01 (w/FP)	X4E@ V X4EFF@ V

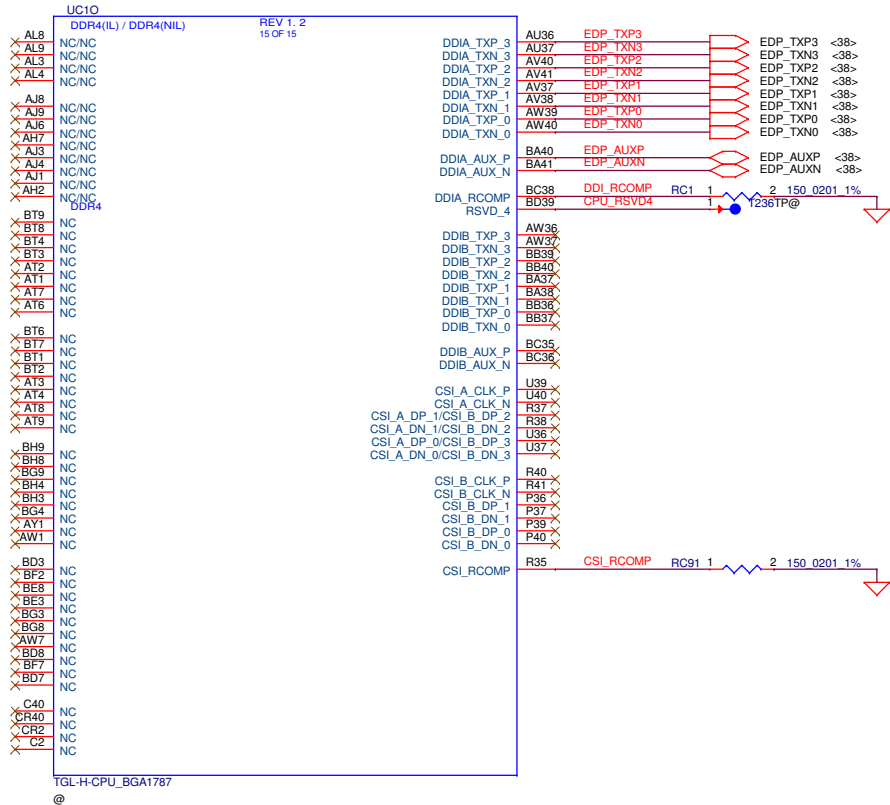
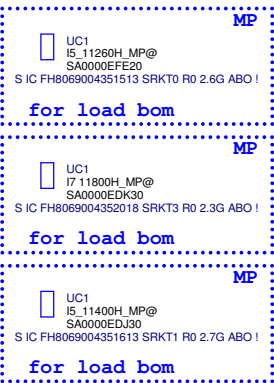
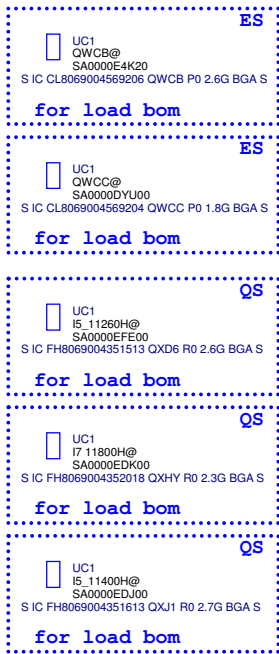
435P4RBOL01(IO/B)
X4EP4RBOL01(IO/B)

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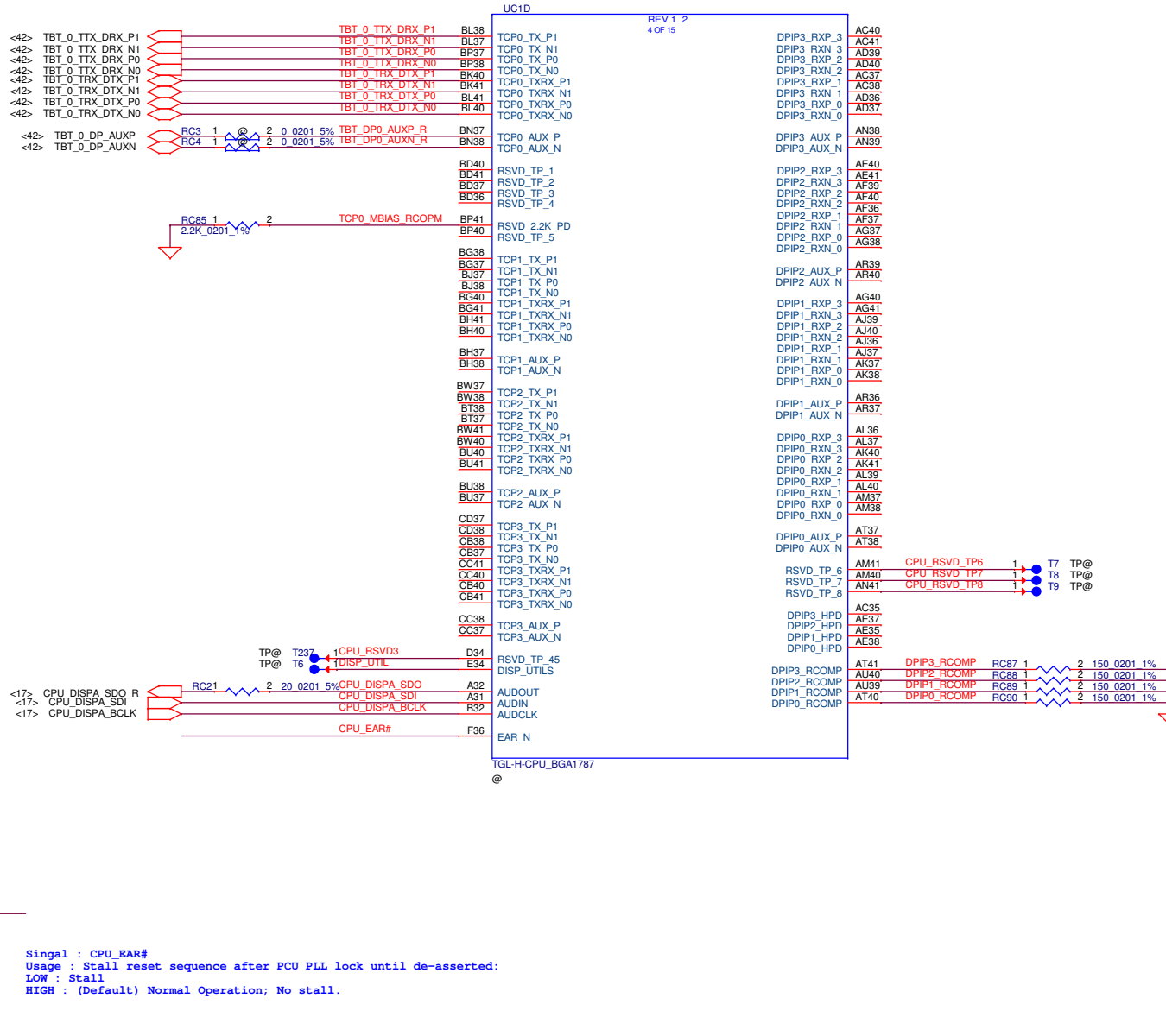
X76869BOLA3 - HYNIX 6G	X76E3_HYN@	E3
X76869BOLA4 - SAMSUNG 6G	X76E3_SAM@	
X76869BOLA5 - HYNIX 8G	X76E5_HYN@	E5/E7
X76869BOLA6 - SAMSUNG 8G	X76E5_SAM@	
X76869BOLA9 - ON OVRR	X76_ON@	OVRR
X76869BOLA9 - uPI OVRR	X76_UPI@	

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				2021/08/06	
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				Notes List	
				Size	Docu
				Date	CH51M MB LA-862P
				Created	Wgjin, 19/12/2021
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BIOS ver: V0.02W1
EC: ver: V002AT04



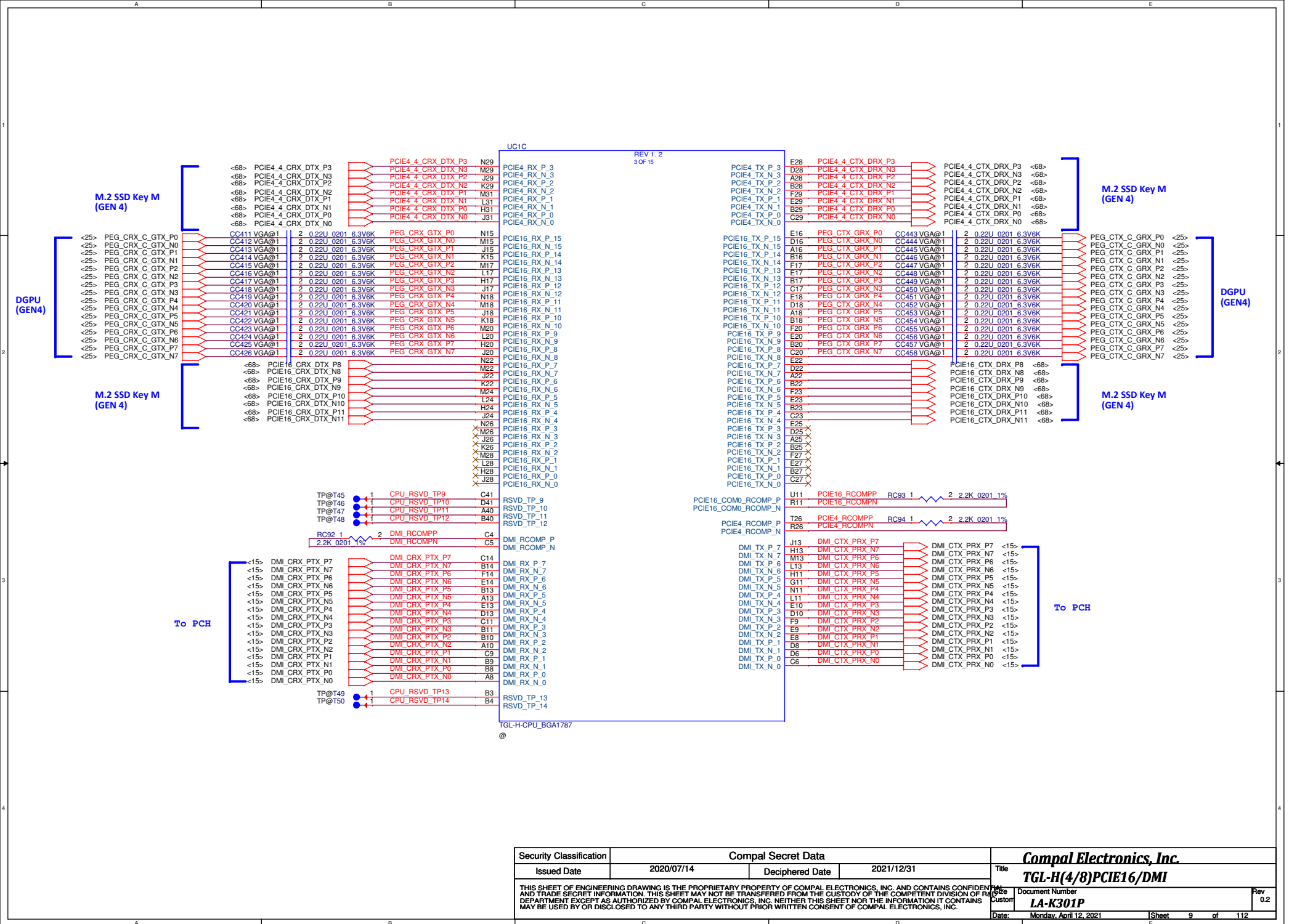
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Issued Date	2020/07/14	Deciphered Date	2021/12/31	TGL-H(1/8)DDI/CSI/Memory	
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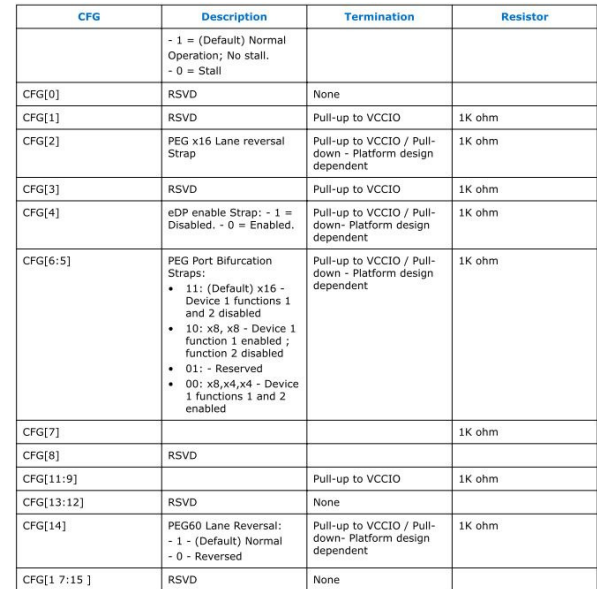
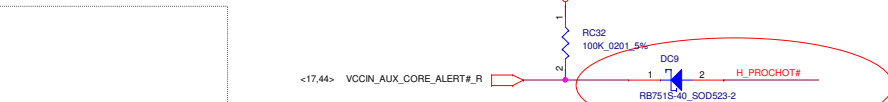
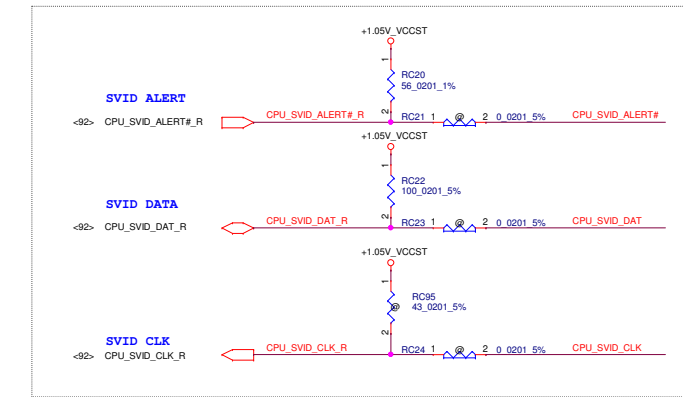
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Interleaved Memory

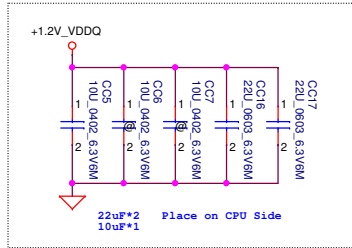
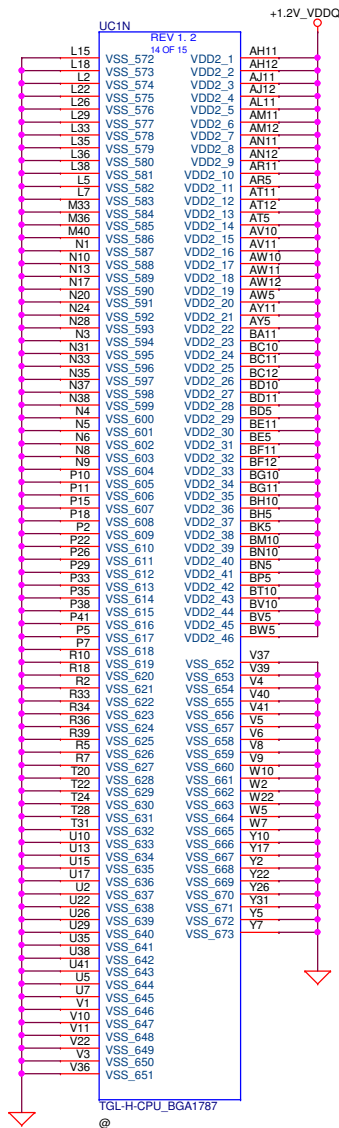




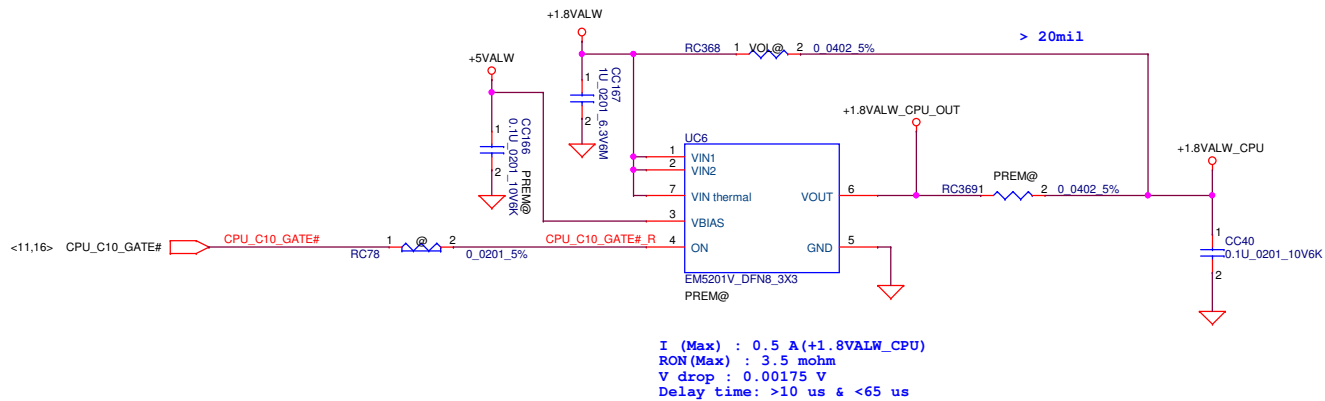
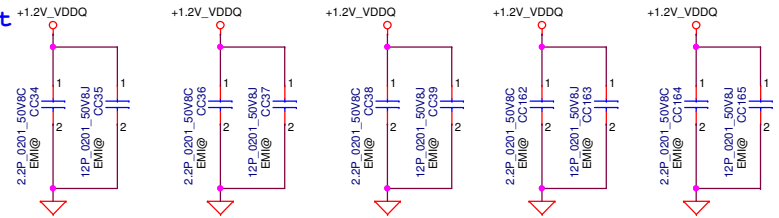
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Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	
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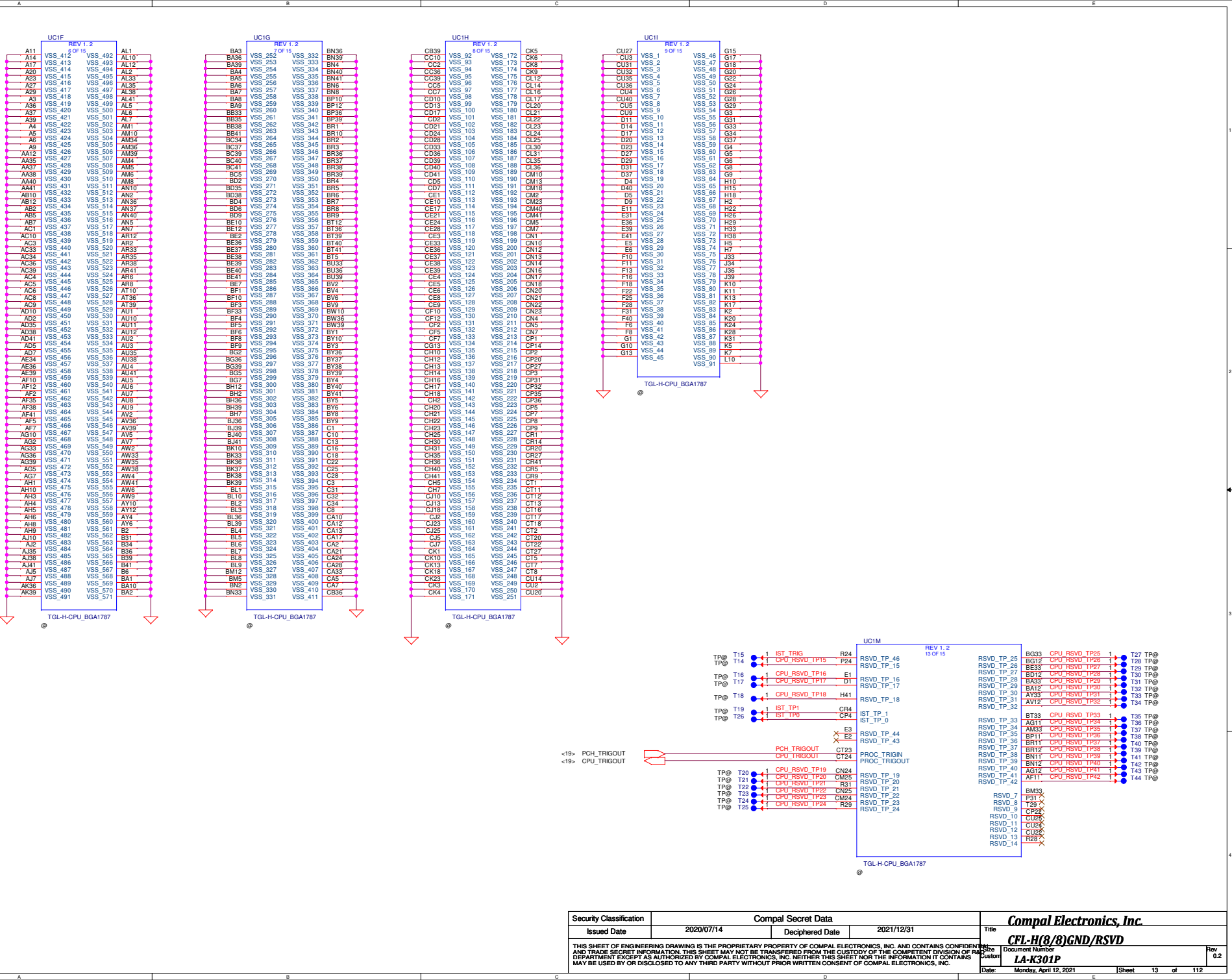
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Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	
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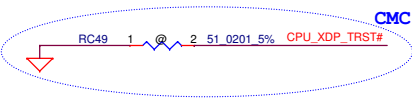
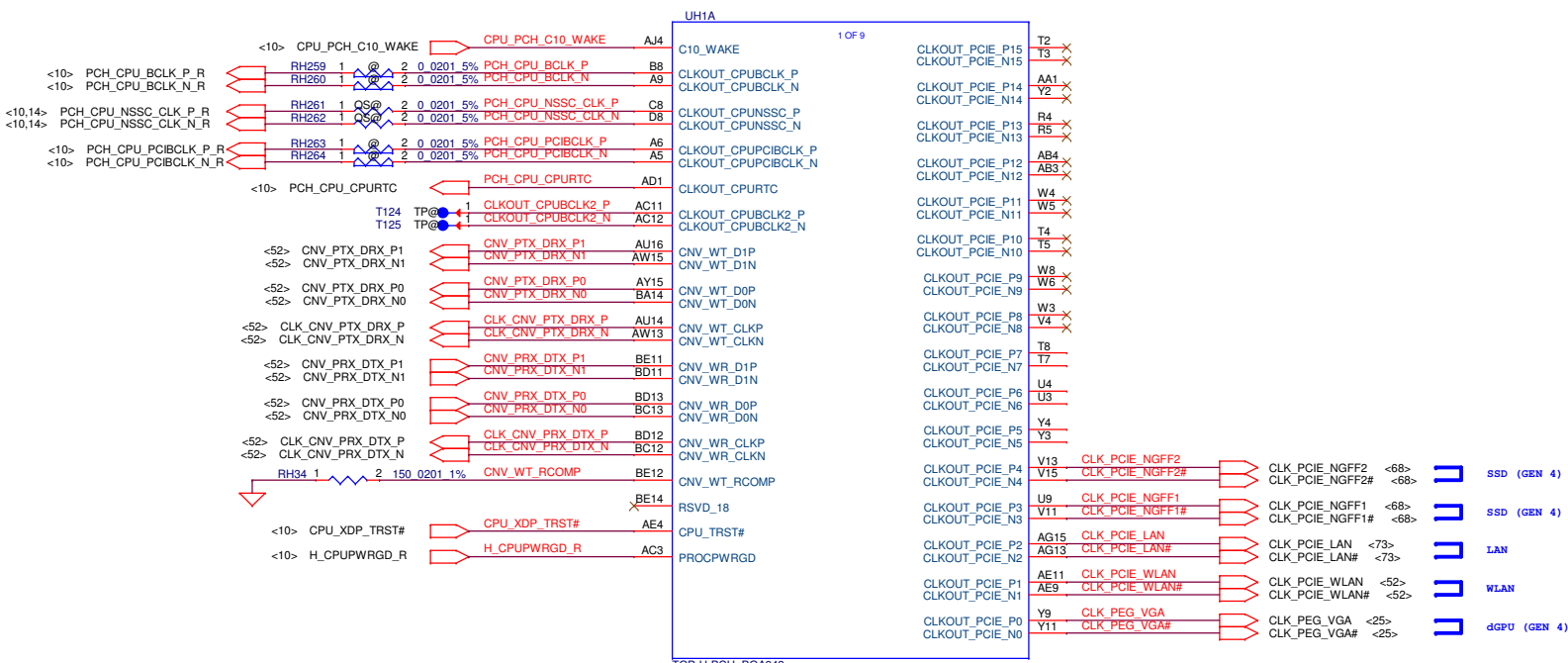
EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



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ES2
UH1 PCH_ES@
TGP-H-PCH_BGA943
SA0000D3F50
for load bom

QS
UH1 PCH_B0@
S IC FH82HM570 QWC2 B0 FCBGA943P PCH-H S
SA0000EDM00
for load bom

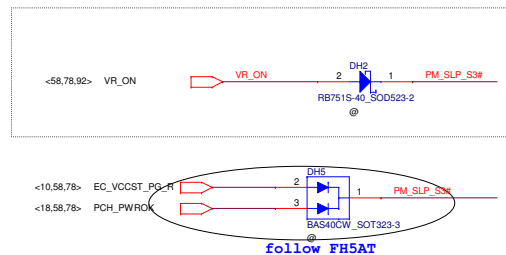
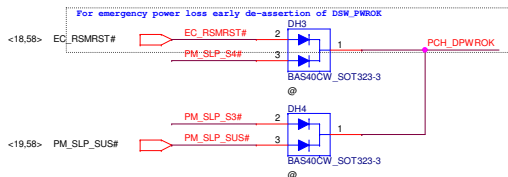
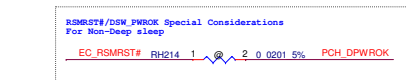
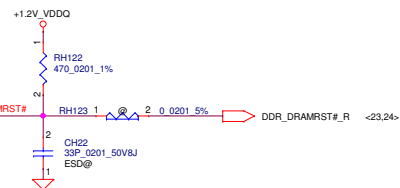
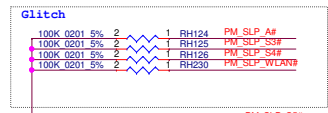
QS
UH1 PCH_B1@
S IC FH82HM570 QX04 B1 FCBGA943P PCH-H S
SA0000EDM10
for load bom

MP
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for load bom

Table 65. Platform Clocks and Associated Signal Details and Descriptions

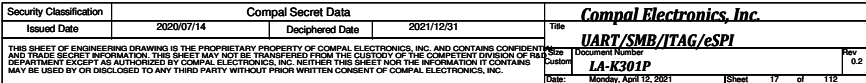
Signal Name	Type	SSC Capable	Description
CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC_N	O	No	Filtered Crystal Reference Clock to CPU: 24MHz differential, filtered crystal reference clock to the processor
CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK_N	O	Yes	Differential Clock to CPU: Reference clock to the processor 100-MHz differential core
CLKOUT_CPUPCIBCLK_P CLKOUT_CPUPCIBCLK_N	O	Yes	Differential PCIe* Reference Clock to CPU: 100-MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	PCI Express* Clock Output: PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices. • CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

continued...



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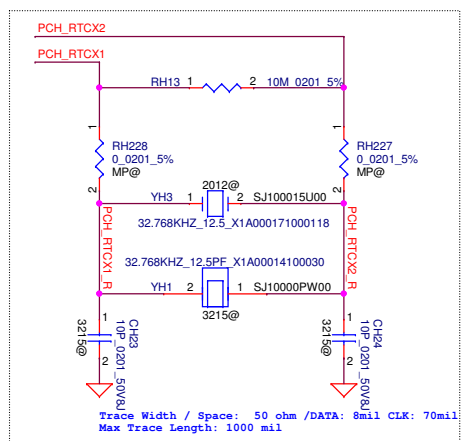


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<10> XDP_PREQ#
<10> H_PM_SYNC_R
<10> H_PM_DOWN_R
<10> H_PLTRST_CPU#
<10,58> H_PECI

1K 0201 5% 2
1K 0201 5% 2

HDD

<67> SATA_PTX_DRX_P2
<67> SATA_PTX_DRX_N2
<67> SATA_PRX_DTX_P2
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CH24 2012@
18P_0201_25V8J
SE000004H00
CH23 2012@
20P_0201_25V8J
SE000002T00

		CL	Package	CH23	CH24	RH13	BOM
SJ10000PW00	S CRYSTAL 32.768KHZ 9PF X1A000141000200	9pF	YH1-3215	10pF (SE173100J80)	10pF (SE173100J80)	10M ohm (SD000012E80)	3215@
SJ100015U00	32.768KHZ 12.5 PF 2012 size_X1A000171000118	12.5pF	YH3-2012	20pF (SE000002T00)	18pF (SE000004H00)	10M ohm (SD000012E80)	2012@

Security Classification	Compal Secret Data	
Issued Date	2020/07/14	Deciphered Date
		2021/12/31

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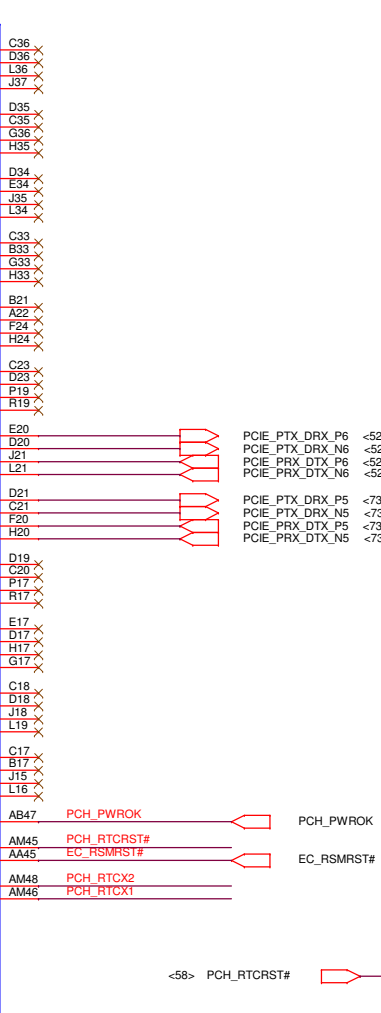
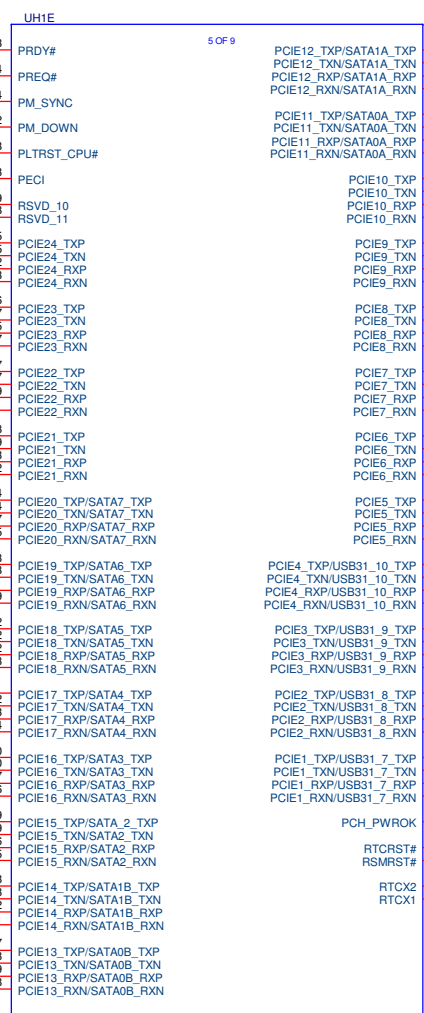
Compal Electronics, Inc.
PCH(5/8)PCIE/SATA

Document Number
LA-K301P

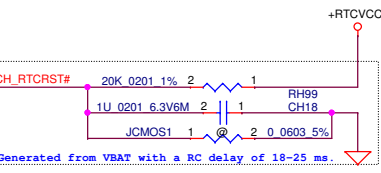
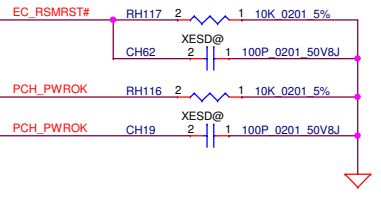
Date: Monday, April 12, 2021

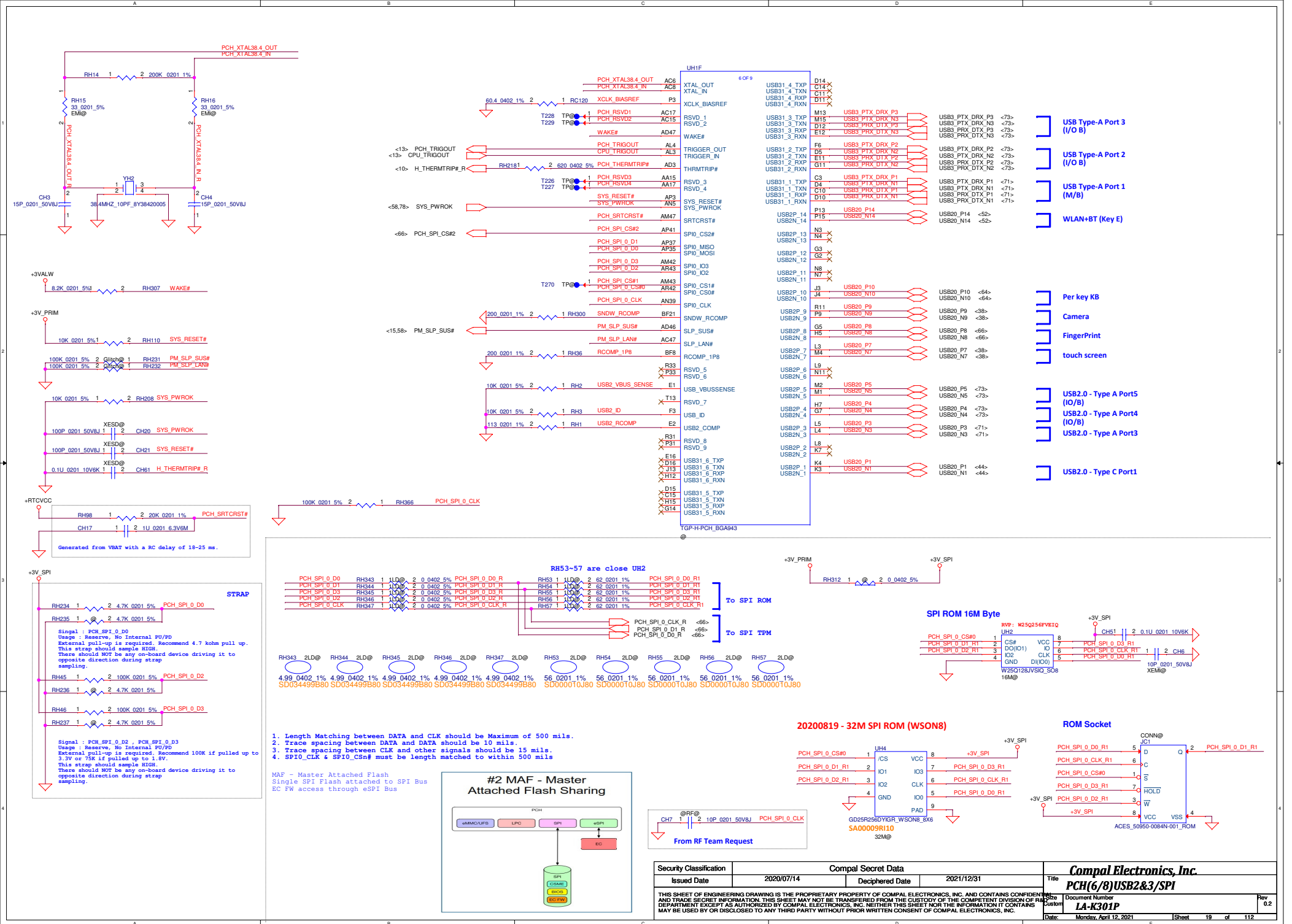
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Rev 0.2



WLAN
LAN





UH1H		
8 OF 9		
A17	VSS_163	AJ23
A2	VSS_164	AJ25
A28	VSS_165	AJ27
A3	VSS_166	AJ28
A33	VSS_167	AK12
A37	VSS_168	AK17
A4	VSS_169	AK18
A41	VSS_170	AK24
A45	VSS_171	AK25
A46	VSS_172	AK26
A47	VSS_173	AK28
A48	VSS_174	AK29
AA12	VSS_175	AK30
AA13	VSS_176	AK32
AA20	VSS_177	AK33
AA22	VSS_178	AK35
AA23	VSS_179	AK38
AA25	VSS_180	AK45
AA29	VSS_181	AK5
AA30	VSS_182	AL19
AA32	VSS_183	AL22
AA33	VSS_184	AL24
AA35	VSS_185	AL25
AA37	VSS_186	AL26
AA49	VSS_187	AL28
AB28	VSS_188	AL29
AC13	VSS_189	AL31
AC18	VSS_190	AM1
AC35	VSS_191	AM12
AC37	VSS_192	AM17
AC4	VSS_193	AM33
AC45	VSS_194	AM35
AC5	VSS_195	AM38
AC9	VSS_196	AM49
AD11	VSS_197	AN17
AD12	VSS_198	AN19
AD13	VSS_199	AN22
AD15	VSS_200	AN24
AD17	VSS_201	AN25
AD18	VSS_202	AN26
AD28	VSS_203	AN31
AD35	VSS_204	AN33
AD37	VSS_205	AN38
AD45	VSS_206	AP12
AD49	VSS_207	AP17
AD5	VSS_208	AP21
AD6	VSS_209	AP25
AD8	VSS_210	AP26
AD9	VSS_211	AP28
AE12	VSS_212	AP31
AE13	VSS_213	AP33
AE15	VSS_214	AP38
AE17	VSS_215	AP45
AE18	VSS_216	AP5
AE35	VSS_217	AT1
AE37	VSS_218	AT12
AE45	VSS_219	AT17
AE5	VSS_220	AT19
AF28	VSS_221	AT21
AG1	VSS_222	AT22
AG12	VSS_223	AT24
AG17	VSS_224	AT25
AG20	VSS_225	AT26
AG22	VSS_226	AT28
AG23	VSS_227	AT29
AG25	VSS_228	AT31
AG27	VSS_229	AT33
AG28	VSS_230	AT37
AG35	VSS_231	AT49
AG37	VSS_232	AT5
AG49	VSS_233	AU25
AH12	VSS_234	AV11
AH13	VSS_235	AV39
AH15	VSS_236	AV45
AH35	VSS_237	AV5
AH38	VSS_238	AW11
	VSS_239	AW24
		VSS_316

TGP-H-PCH_BGA943
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UH1I		
9 OF 9		
AW25	VSS_1	F42
AW39	VSS_2	F8
AY25	VSS_3	G1
AY43	VSS_4	G41
AY5	VSS_5	G48
AY7	VSS_6	G49
B1	VSS_7	G9
B2	VSS_8	H25
B4	VSS_9	H43
B46	VSS_10	H45
B48	VSS_11	J11
B49	VSS_12	J25
B6	VSS_13	J39
BA41	VSS_14	J9
BA43	VSS_15	K11
BA49	VSS_16	K39
BA9	VSS_17	K45
BB25	VSS_18	K5
BB44	VSS_19	L14
BB8	VSS_20	L25
BC11	VSS_21	M12
BC15	VSS_22	M17
BC19	VSS_23	M19
BC24	VSS_24	M21
BC25	VSS_25	M22
BC26	VSS_26	M24
BC31	VSS_27	M25
BC35	VSS_28	M26
BC39	VSS_29	M28
BC41	VSS_30	M29
BC9	VSS_31	M31
BF1	VSS_32	M33
BF13	VSS_33	M38
BF2	VSS_34	M49
BF42	VSS_35	M5
BF49	VSS_36	P12
BG17	VSS_37	P21
BG2	VSS_38	P24
BG22	VSS_39	P25
BG25	VSS_40	P28
BG28	VSS_41	P38
BG33	VSS_42	P4
BG37	VSS_43	P45
BG41	VSS_44	P5
BG48	VSS_45	R21
BG9	VSS_46	R24
C1	VSS_47	R25
C12	VSS_48	R28
C24	VSS_49	T1
C4	VSS_50	T12
C49	VSS_51	T15
C7	VSS_52	T17
D1	VSS_53	T33
D13	VSS_54	T38
D2	VSS_55	T49
D24	VSS_56	U19
D25	VSS_57	U21
D33	VSS_58	U22
D37	VSS_59	U24
D49	VSS_60	U25
D7	VSS_61	U26
E13	VSS_62	U28
E15	VSS_63	U29
E19	VSS_64	U31
E22	VSS_65	V12
E24	VSS_66	V17
E25	VSS_67	V21
E26	VSS_68	V22
E31	VSS_69	V24
E33	VSS_70	V25
E35	VSS_71	V26
E37	VSS_72	V33
E39	VSS_73	V38
E9	VSS_74	V5
F25	VSS_75	W27
	VSS_76	W28
	VSS_77	W30
		W44
		Y12
		Y13
		Y15
		Y17
		Y18
		Y32
		Y38
		Y38
		VSS_162

TGP-H-PCH_BGA943
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Reserve Page

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				Date:	Monday, April 12, 2021	Sheet 22 of 112

> Non-ECC SO-DIMM



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Date:	Monday, April 12, 2021		J'Sent 23 of 112		

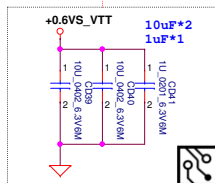
> Non-ECC SO-DIMM



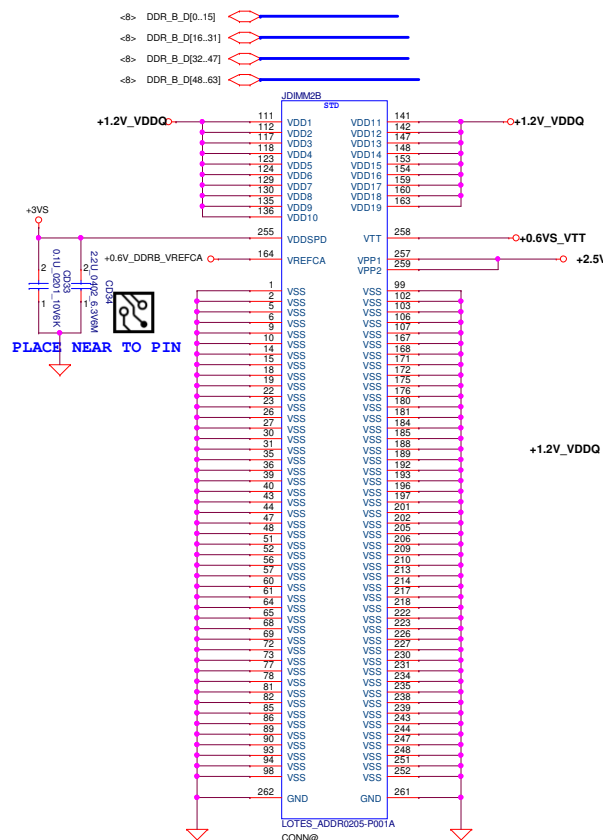
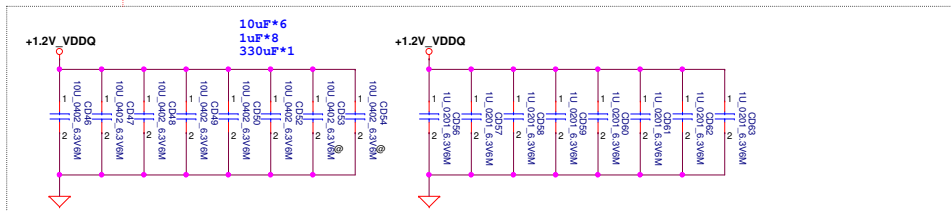
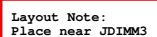
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM3.257,259

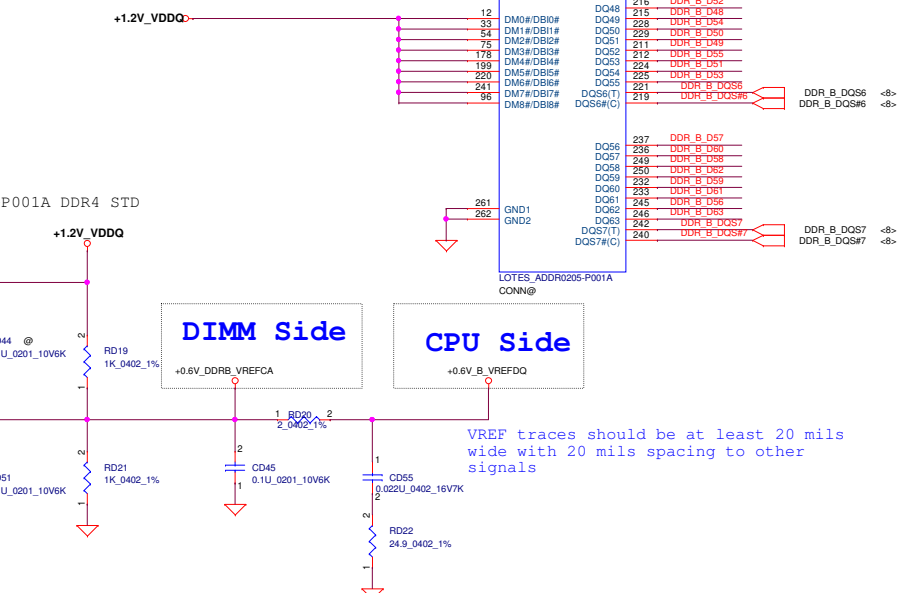
Layout Note:
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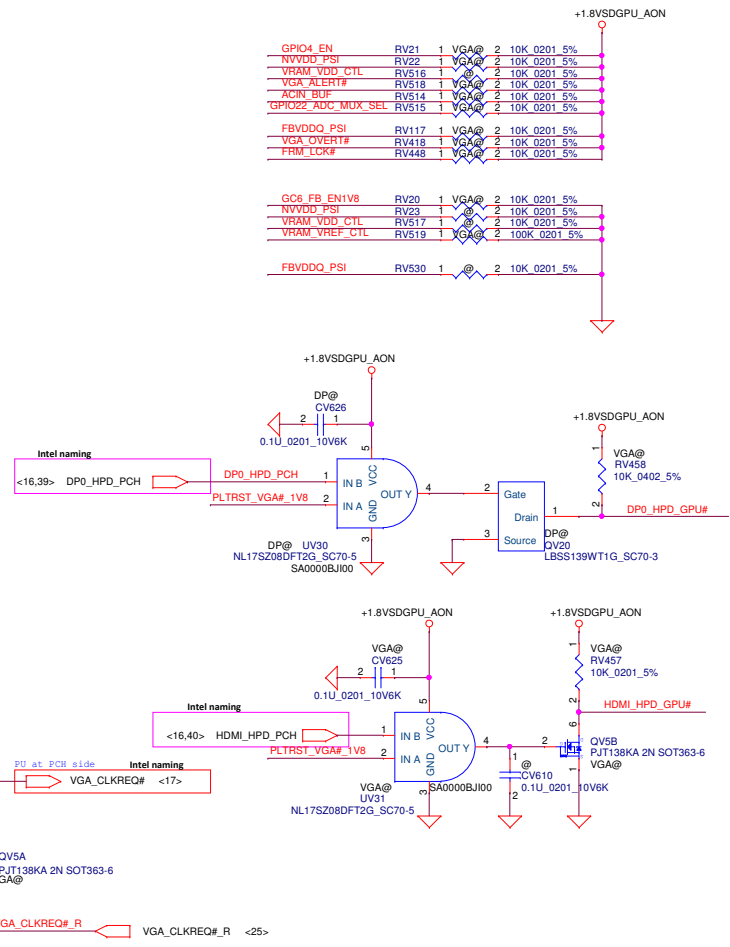
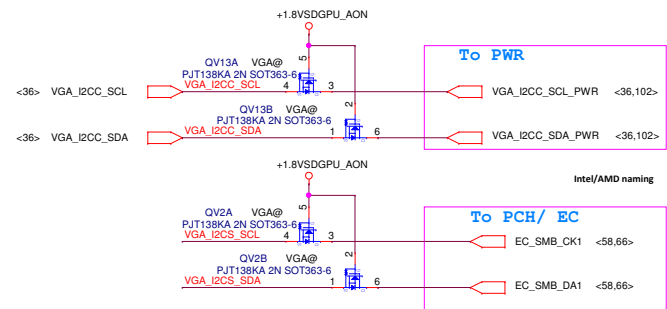
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



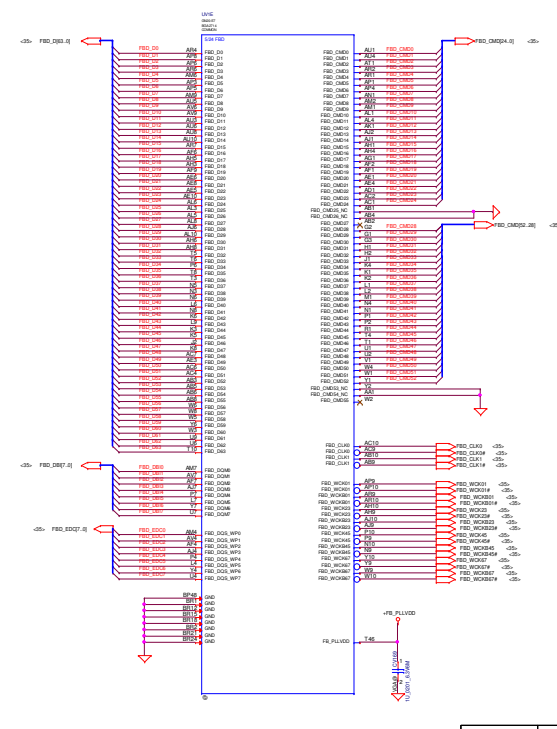
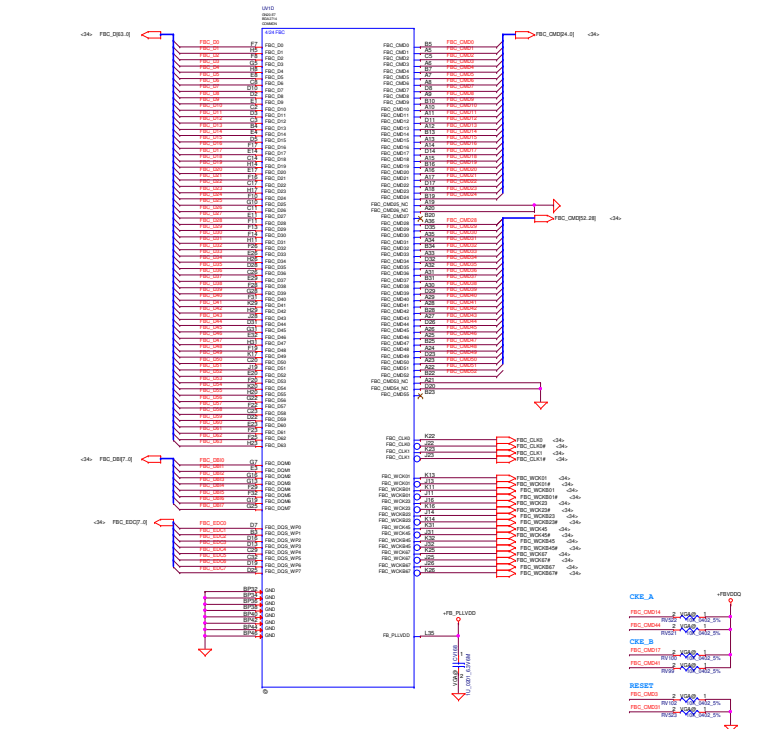
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD

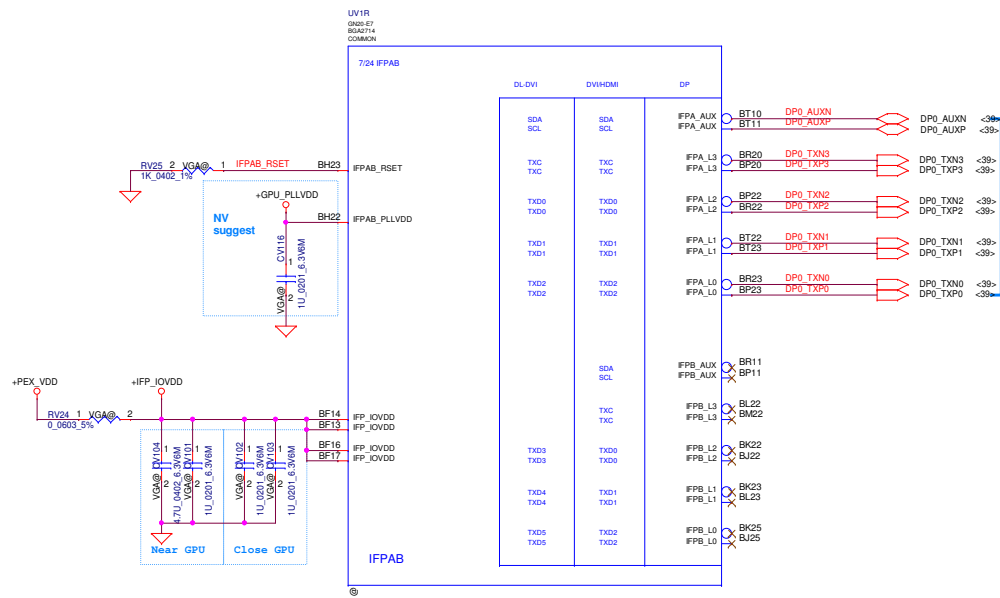


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					GH51M MB LA-J862P	0.1
				Date:	Monday, April 12, 2021	Sheet 24 of 112

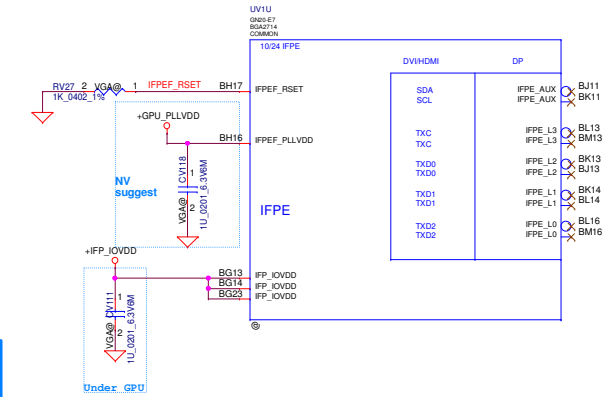


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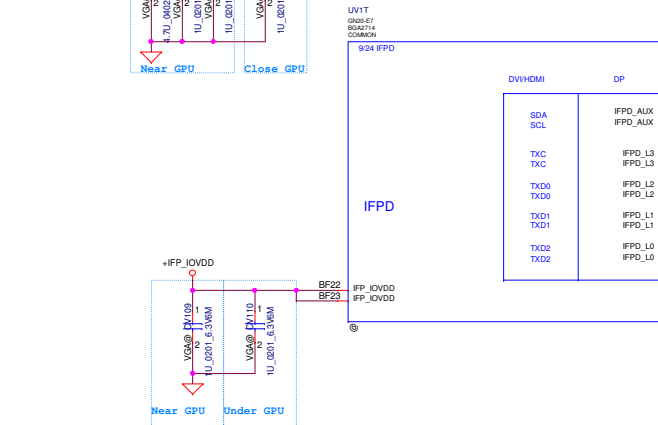
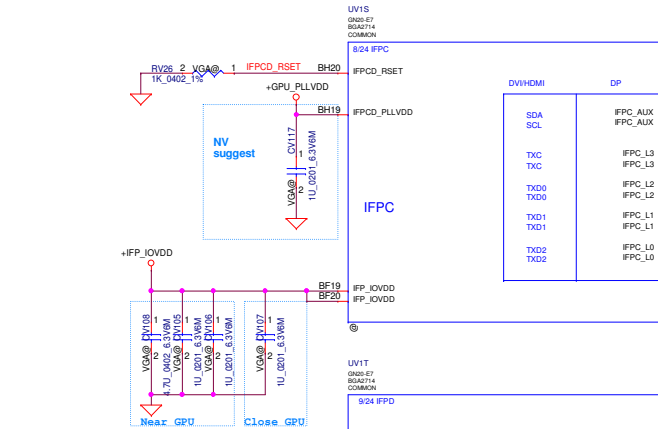
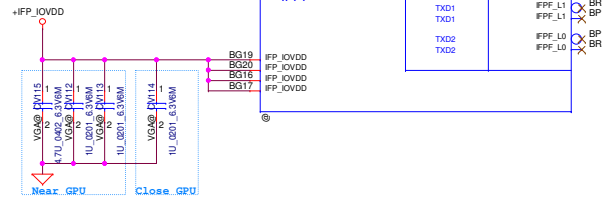




mDP

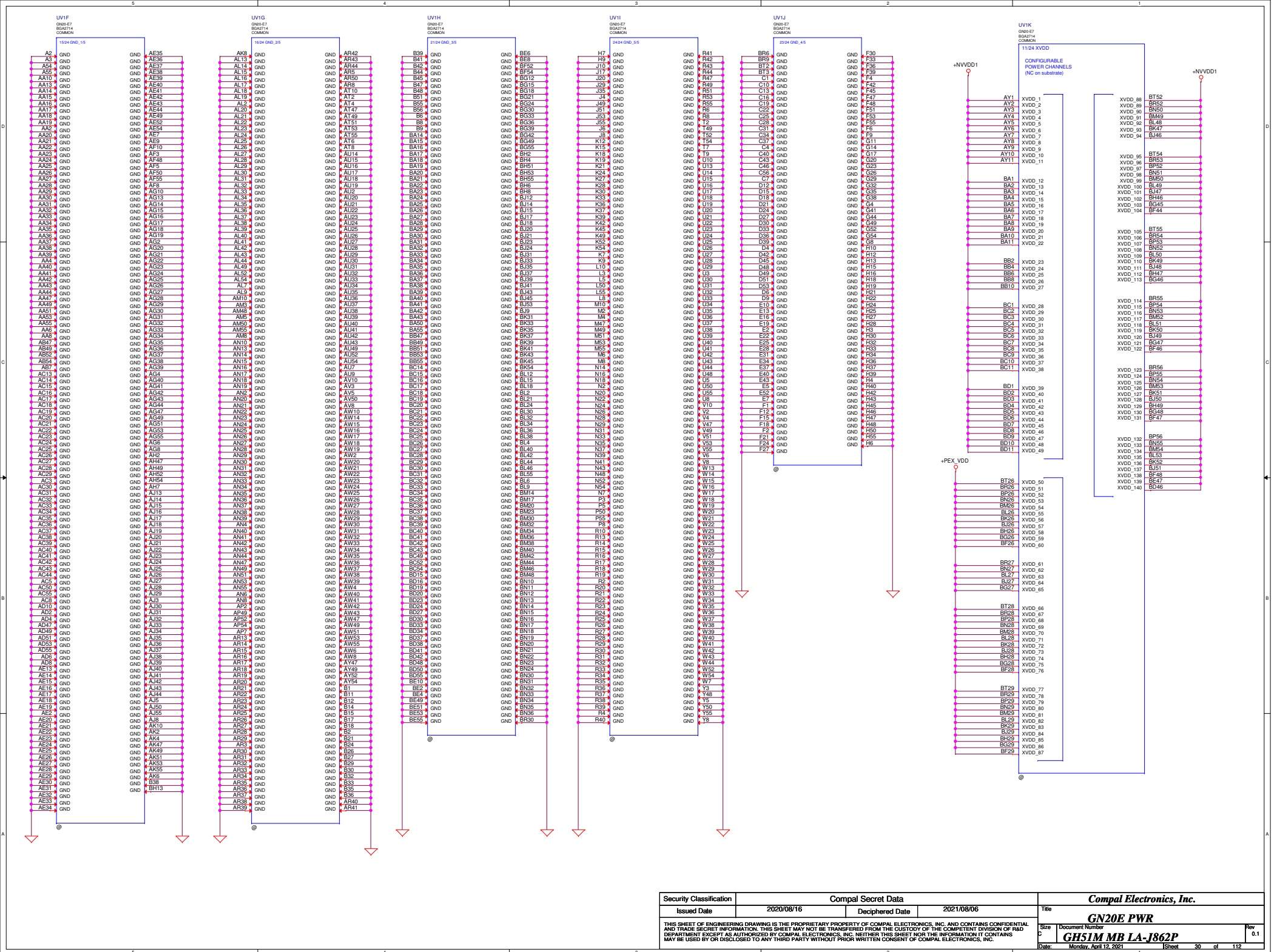


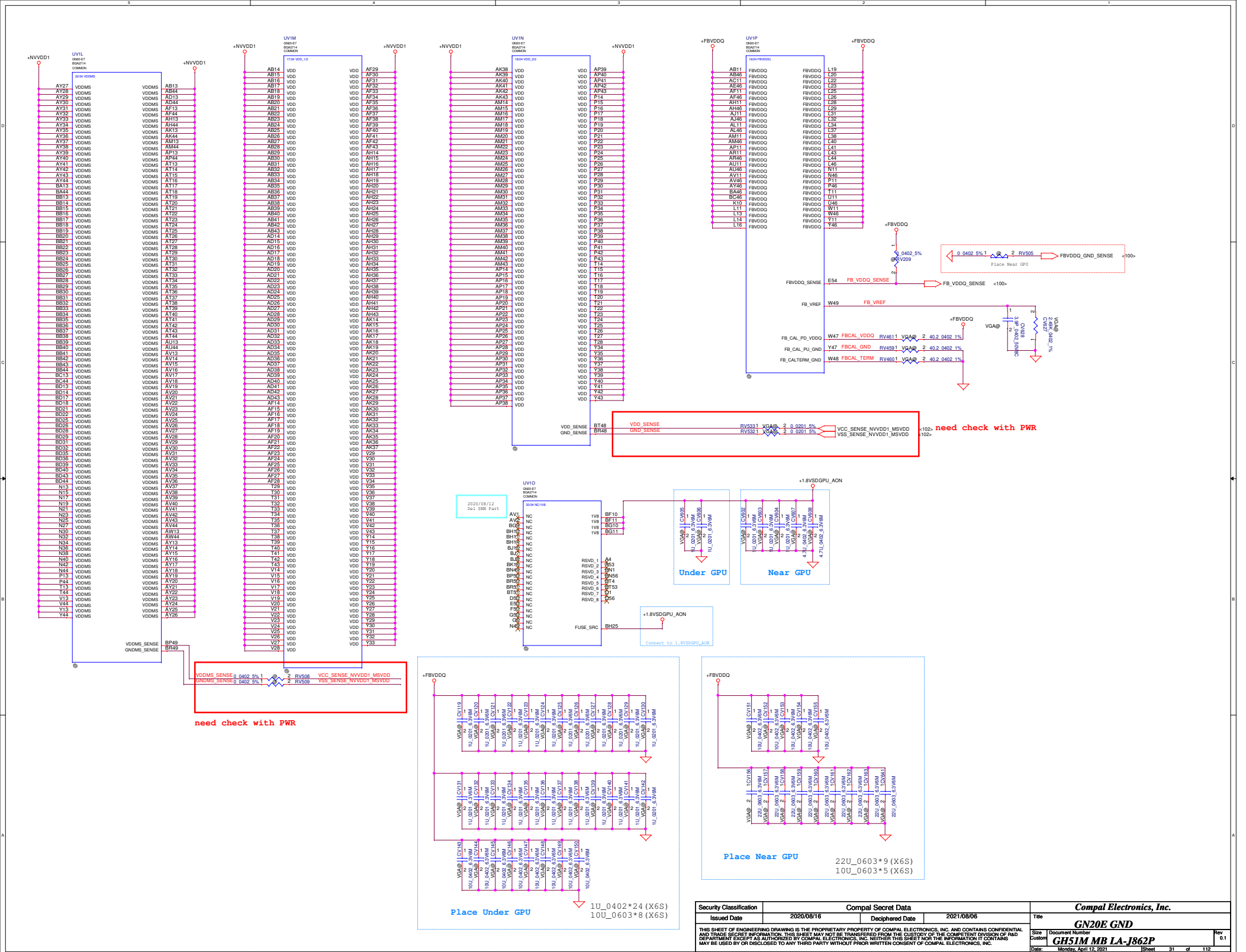
HDMI 2.1



Rename for HDMI
2020/08/18

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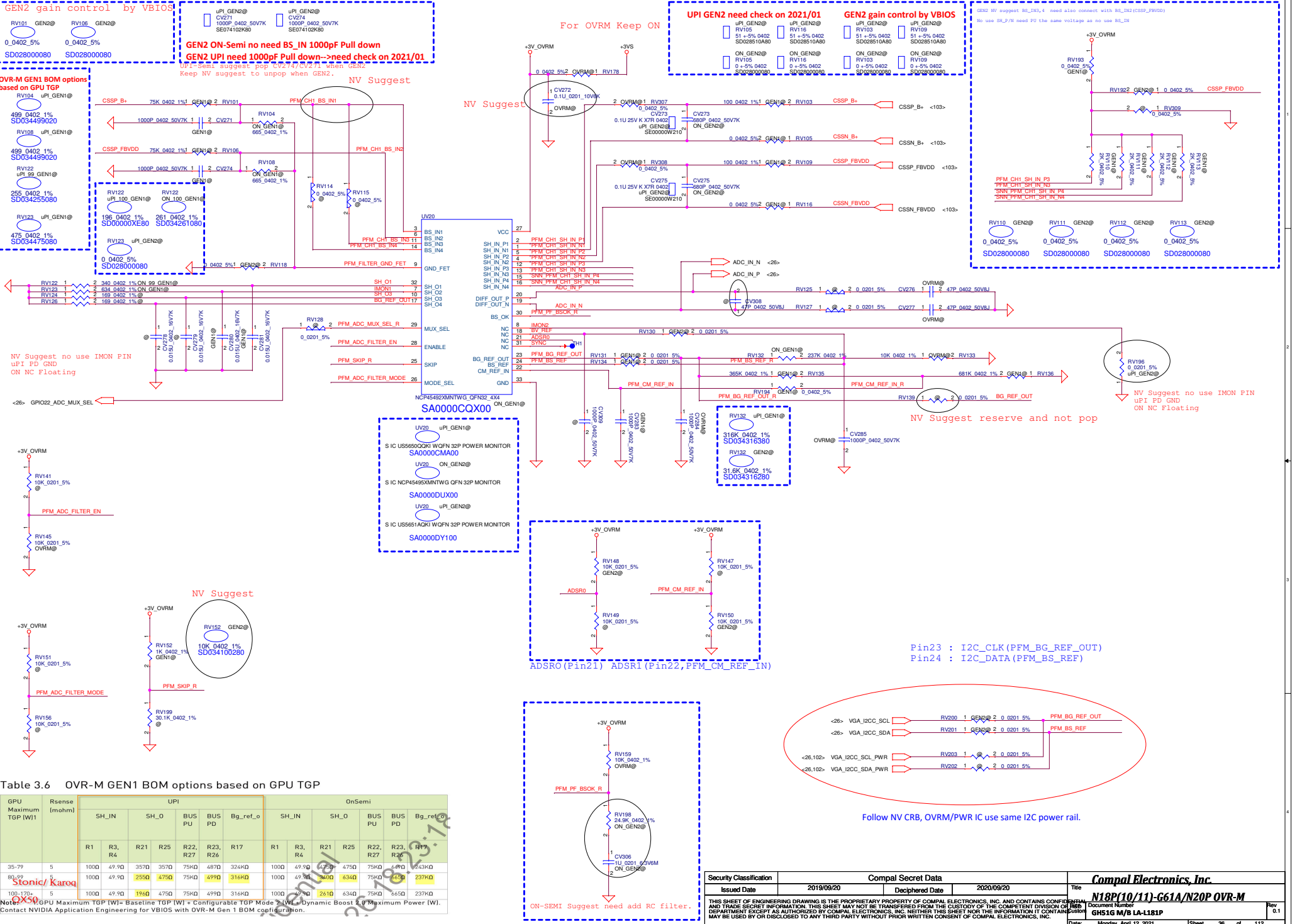
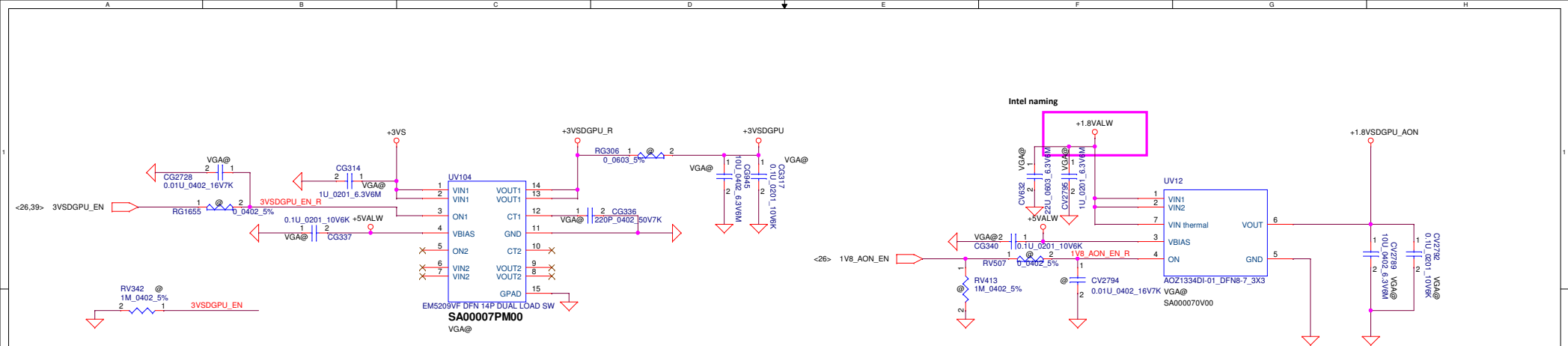
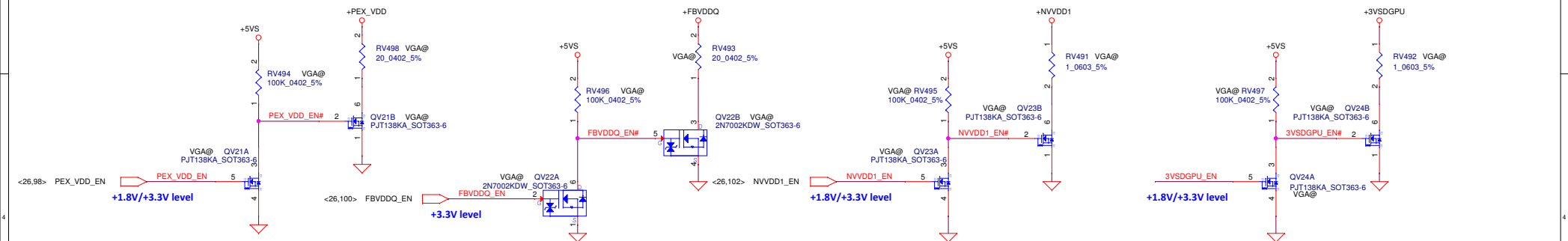


Table 3.6 OVR-M GEN1 BOM options based on GPU TGP															
GPU Maximum TGP (W)	Rsense (mohm)	UPLI							OnSemi						
		SH_IN		SH_O	BUS PU	BUS PD	Bg_ref_o	SH_IN		SH_O	BUS PU	BUS PD	Bg_ref_o		
		R1	R3, R4	R21	R25	R22, R27	R23, R26	R17	R1	R3, R4	R21	R25	R22, R27	R23, R26	R17
35-79	5	1000	49.9K	3570	3570	75K	4870	324K	1000	49.9K	1950	4750	75K	4870	324K
80-99	5	1000	49.9K	2550	4750	75K	4990	316K	1000	49.9K	1950	4750	75K	4870	324K
100-170	5	1000	49.9K	1950	4750	75K	4990	316K	1000	49.9K	1950	4750	75K	4870	324K

Note: GPU Maximum TGP (W) = Baseline TGP (W) + Configurable TGP Mode 2 (W) + Dynamic Boost 2.0 (W) + Maximum Power (W).
Contact NVIDIA Application Engineering for VBIOS with OVR-M Gen 1 BOM configuration.

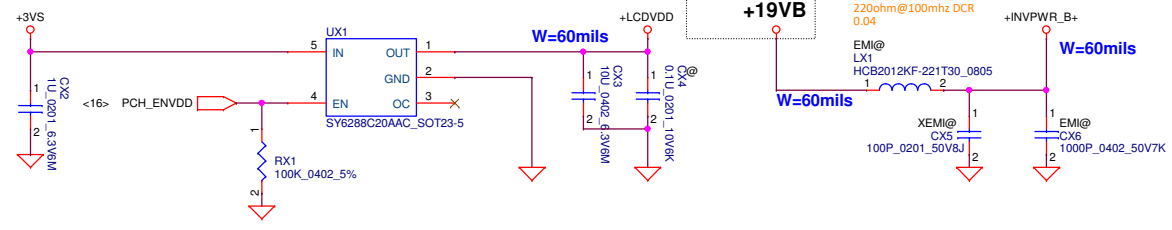


For Power down sequence

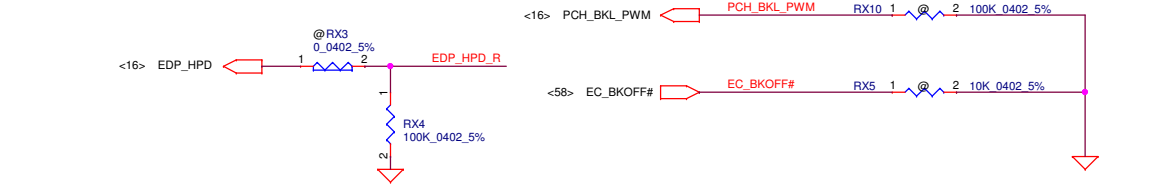


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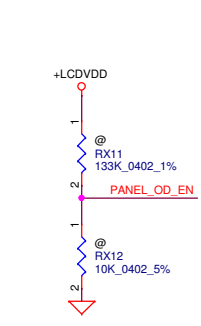
LCD POWER CIRCUIT



LCD enable signal

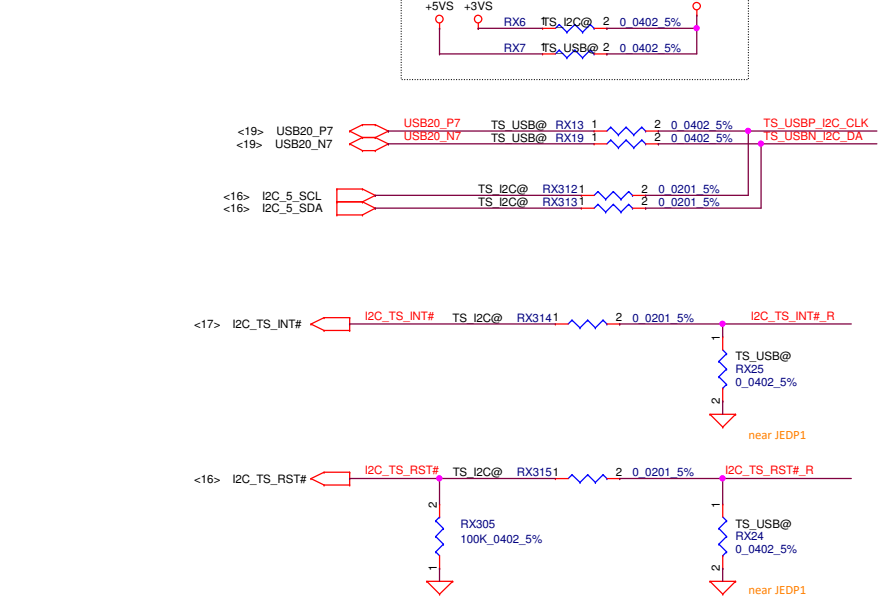


Panel OD

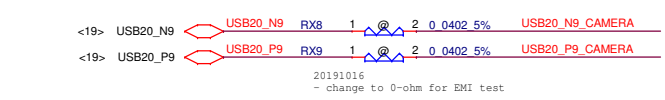


20191209
- RX11 change to unpop
- BIOS needs to detect panel
to select H or L.

USB/I2C Touch Screen Co-Lay

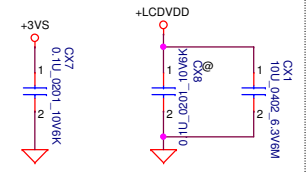


CAMERA

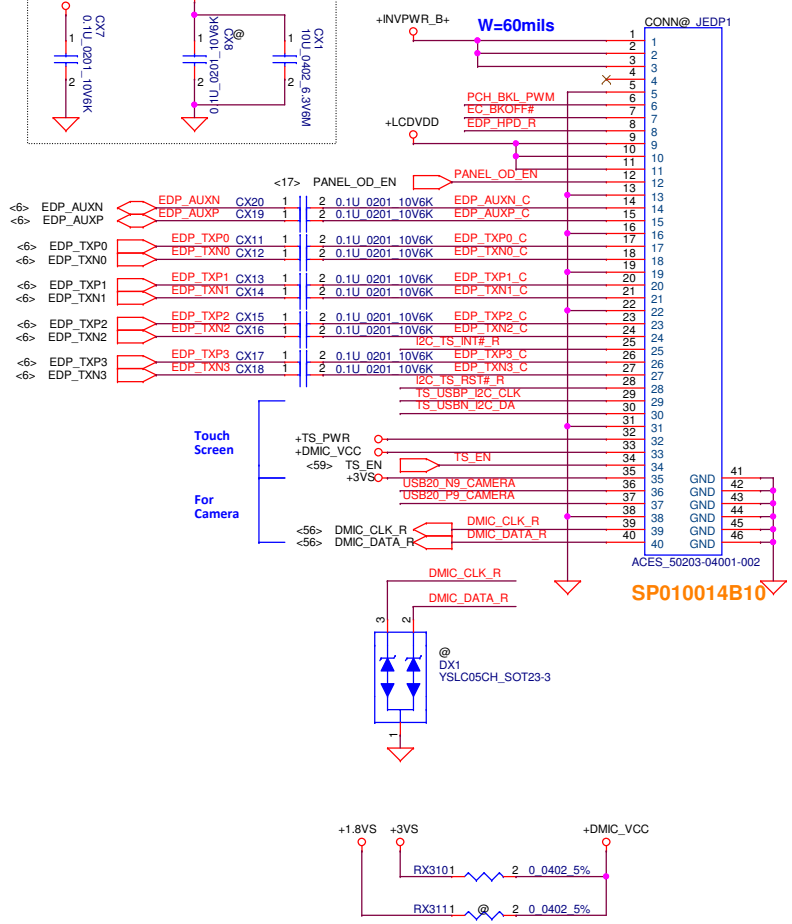


20191016
- change to 0-ohm for EMI test

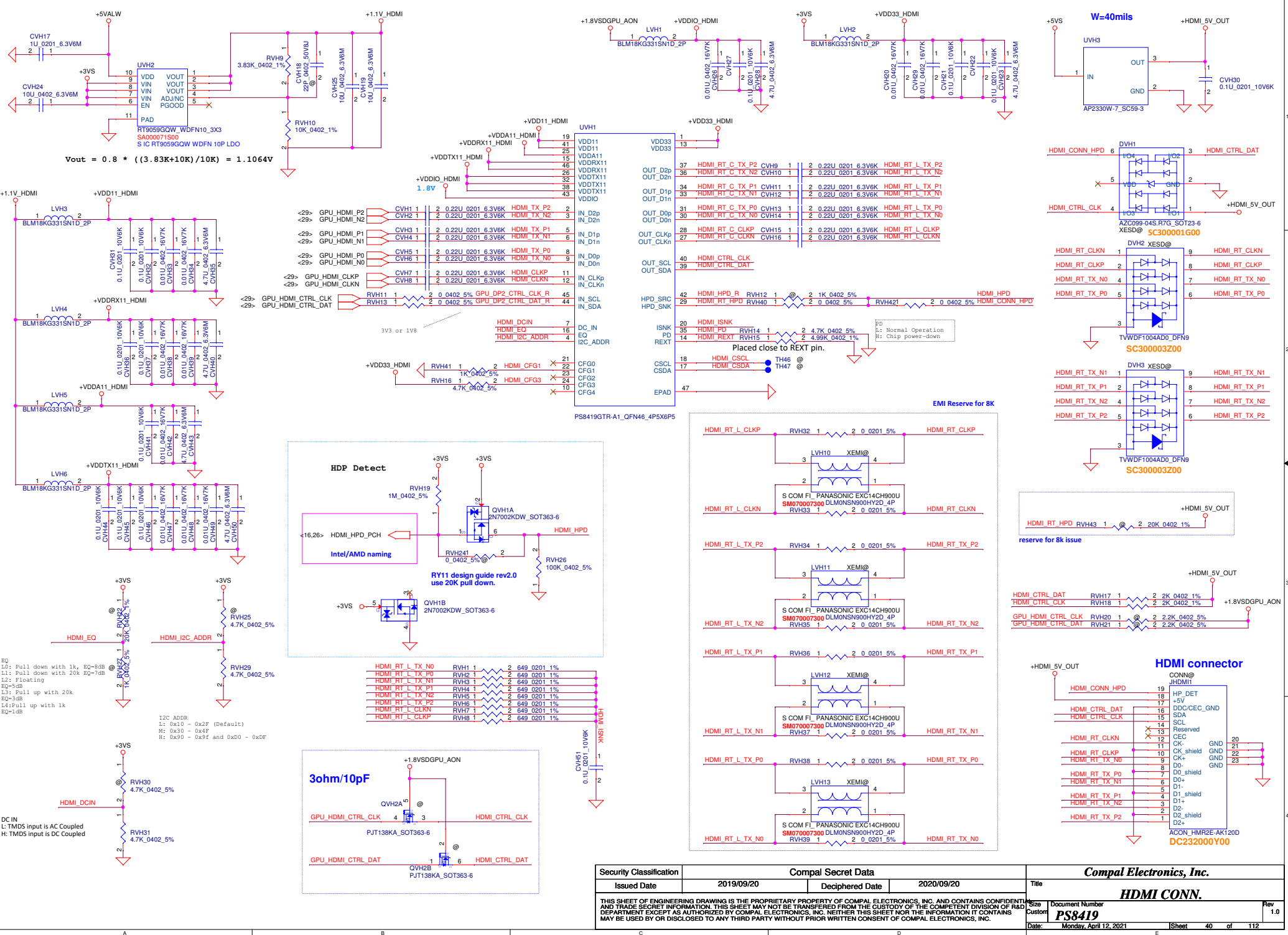
Place closed to JEDP1



LED PANEL Conn.



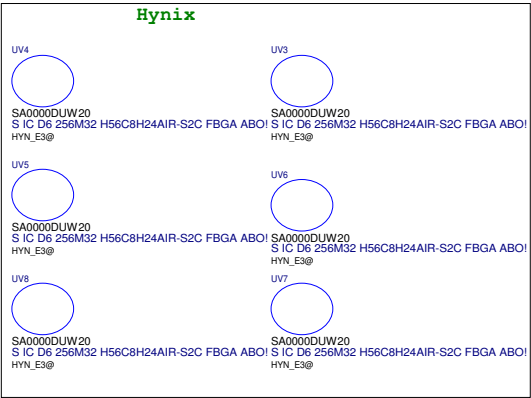
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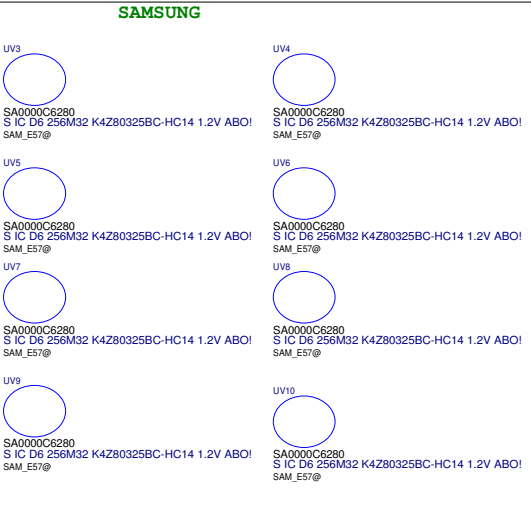
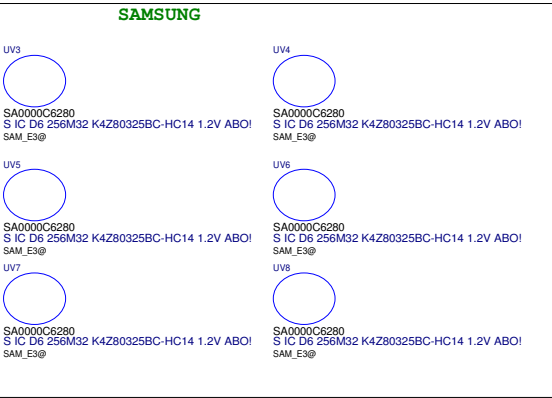
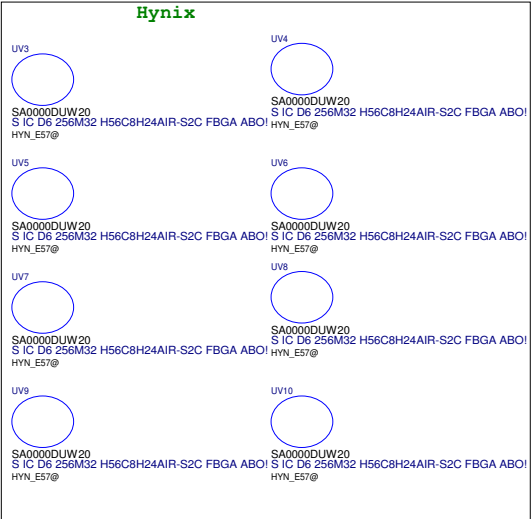
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2019/09/20		2020/09/20		PS8419	
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		Date		Monday, April 12, 2021	
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VRAM

GN20-E3

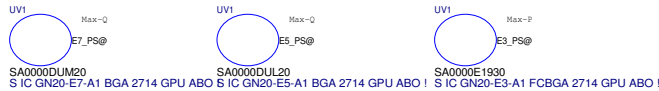


GN20-E5 / E7



GPU

GPU



X76

X76

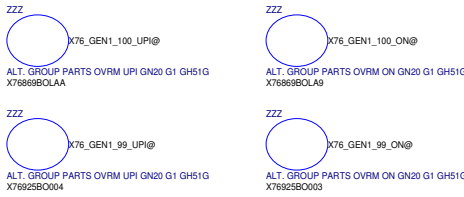
E3 (VRAM*6)



E5 / E7 (VRAM*8)

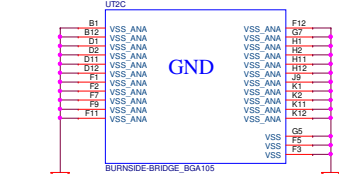
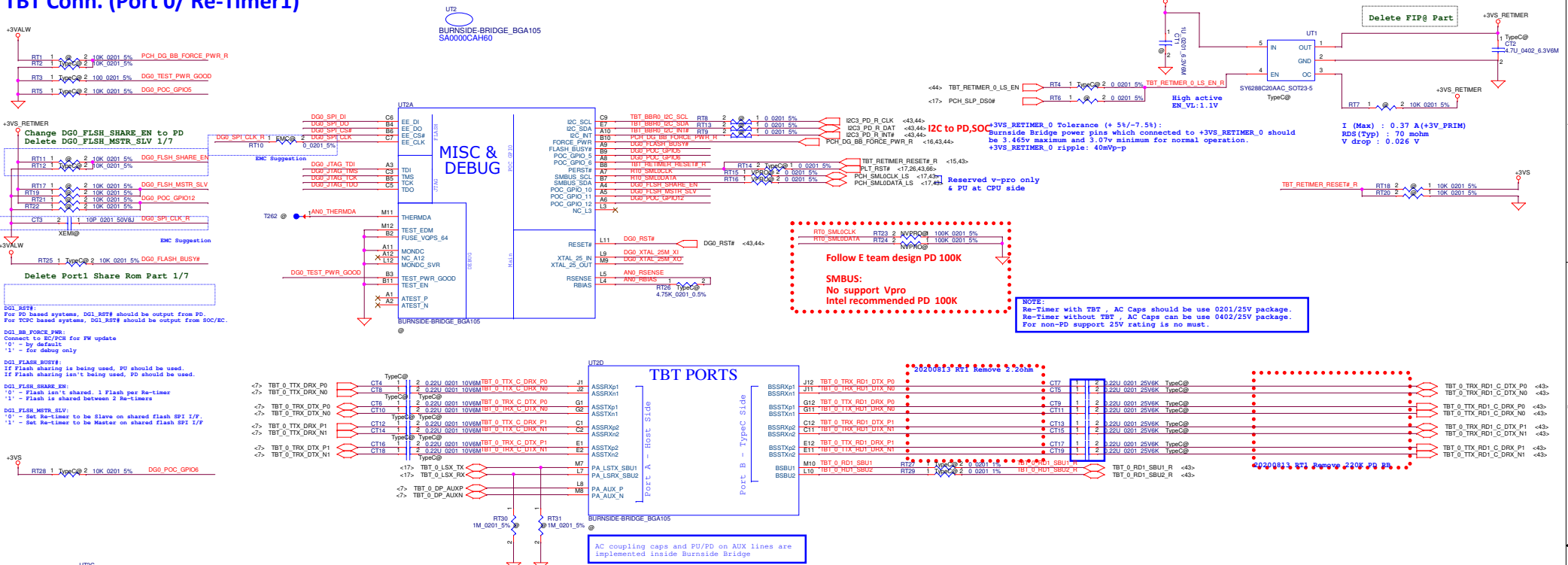


OVRM

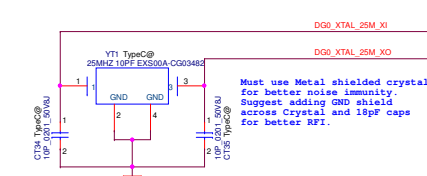


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2020/08/16		2021/08/06		GPU/VRAM/OVRM Config		
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				Date:	Monday, April 12, 2021	Sheet

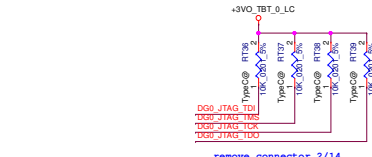
TBT Conn. (Port 0/ Re-Timer1)



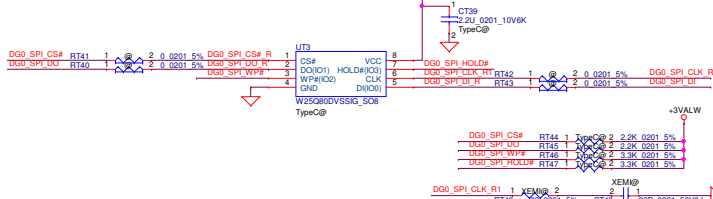
25M XTAL (Type-C Port0)



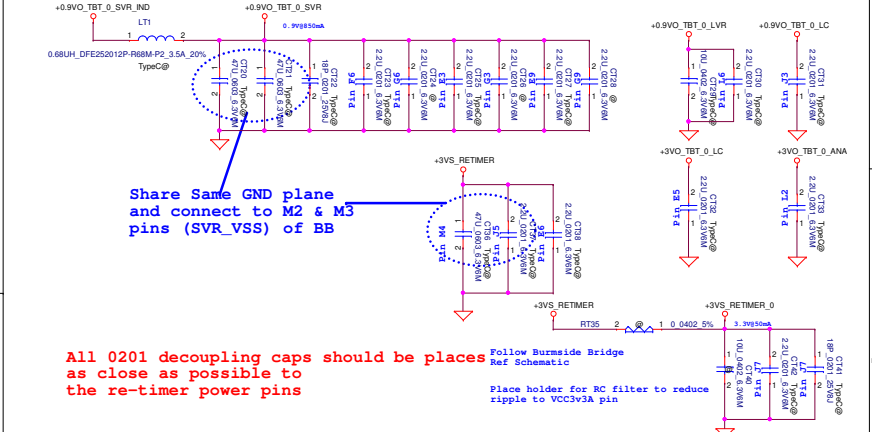
JTAG (Type-C Port0)



SPI ROM (Type-C Port0)

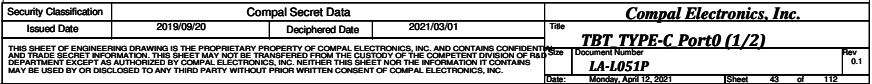


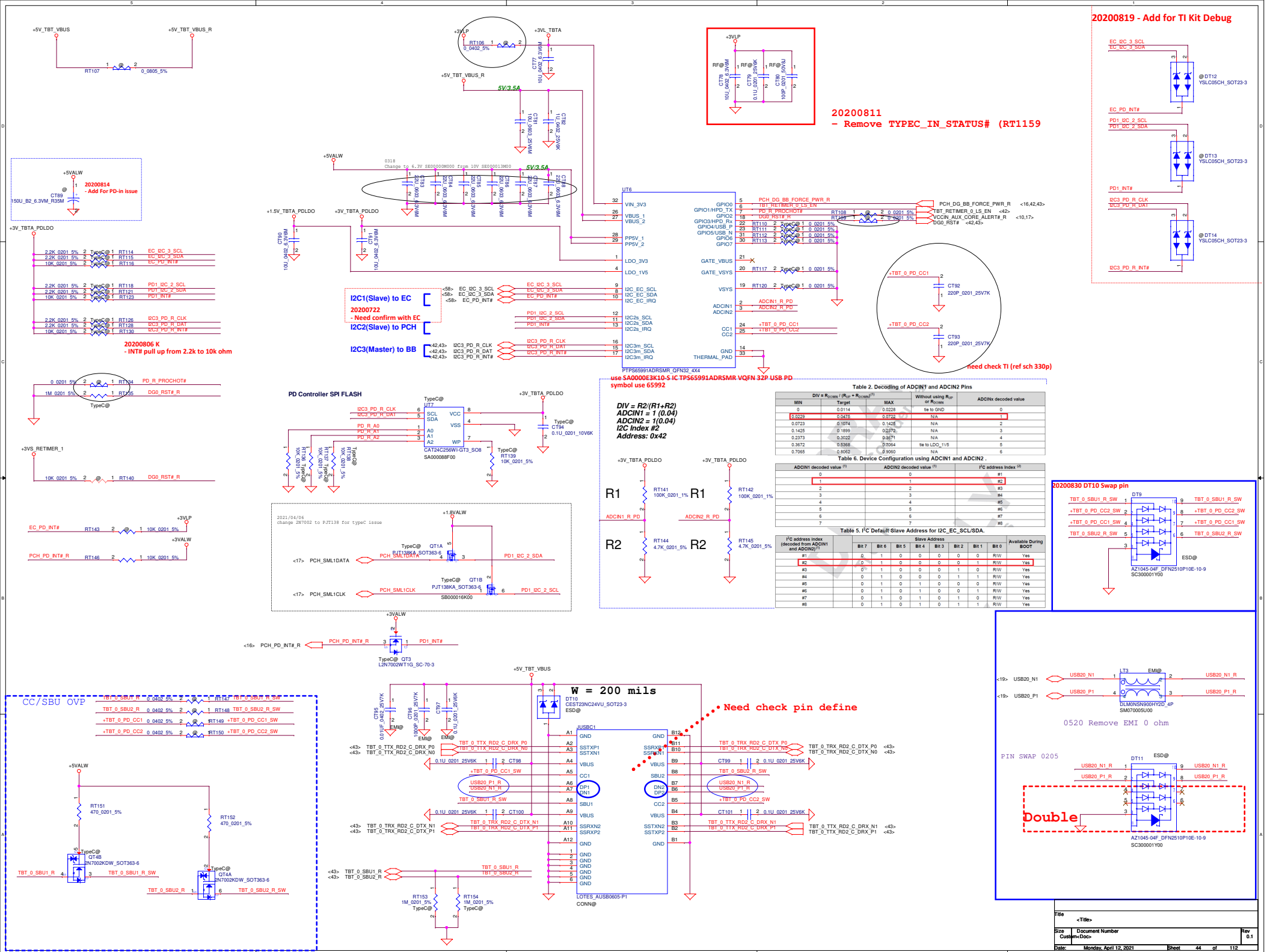
Power Supply Decoupling of Type-C Port0



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SA0000CAH60





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		GH51M MB LA-J862P		0.1	
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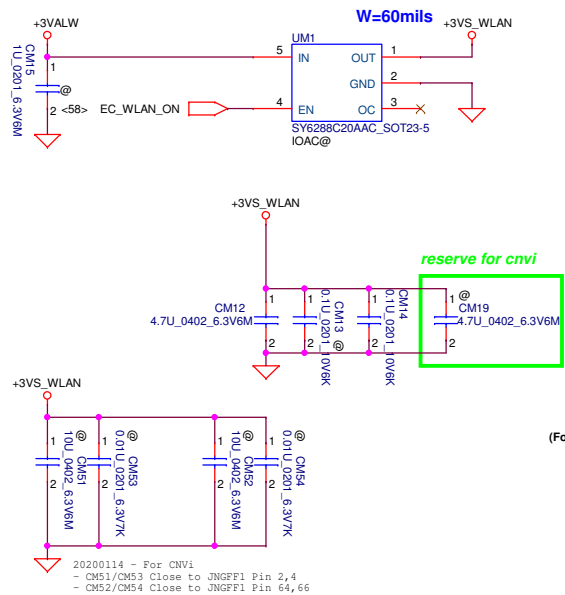
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20190918
LAN more to IO/B

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Wireless LAN

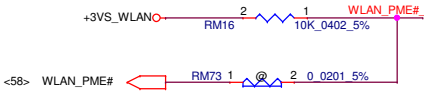


NGFF WL+BT (KEY E)

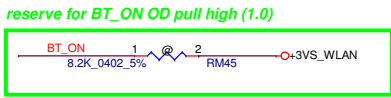
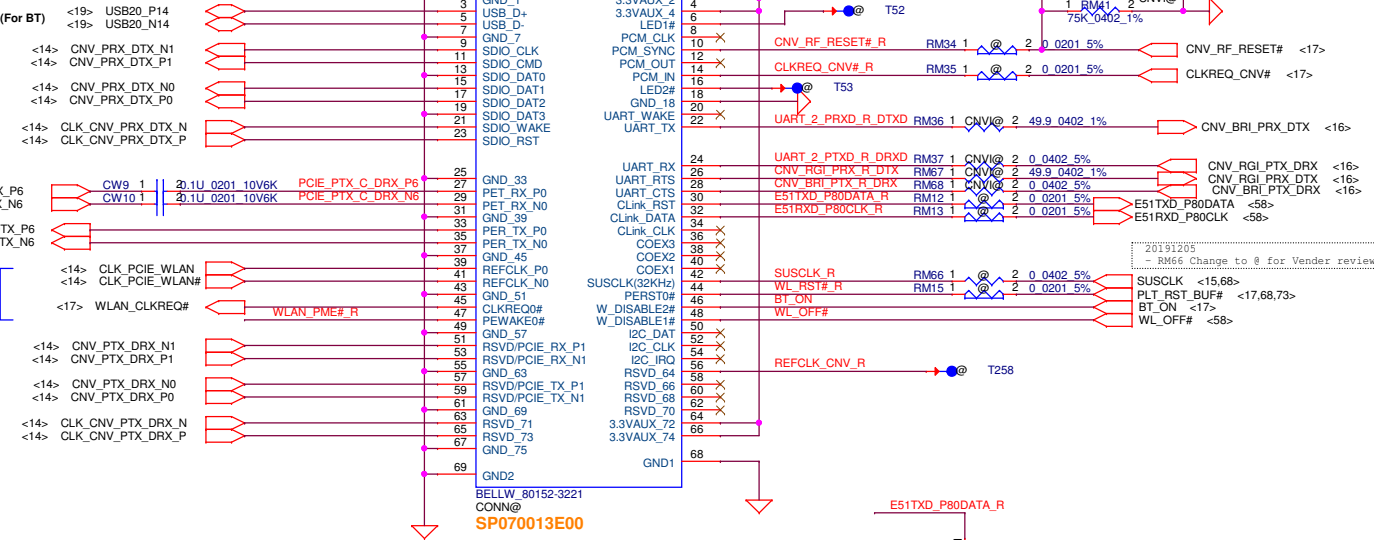
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO/PEWake1#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ#	GND	69
66	UM_SWP/PERST#	Reserved/PETrn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I/O)(3.3)	GND	63
60	OC CLK (O)(0.3.3)	Reserved/PETrn1	61
58	OC DATA (I/O)(0.3.3)	Reserved/PETrn1	59
56	W_DISABLE# (O)(0.3.3V)	GND	57
54	Reserved/W_DISABLE2 (O)(0.3.3V)	PEWakeDr (O)(0.3.3V)	55
52	PERST0# (O)(0.3.3V)	CLKREQ0# (O)(0.3.3V)	53
50	SUSCLK(32KHz) (O)(0.3.3V)	GND	51
48	CODEX1 (I/O)(0.1.8V)	REFCLK0#	47
46	CODEX3 (O)(0.1.8V)	GND	45
44	CODEX3 (O)(0.1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	PERn0	39
38	VENDOR DEFINED	PERp0	37
36	UART RTS (O)(0.1.8V)	PERn0	35
34	UART CTS (I/O)(0.1.8V)	PERp0	33
32	UART TX (O)(0.1.8V)	GND	31
30	UART RX (I/O)(0.1.8V)	GND	29
28	UART Wake# (I/O)(0.3.3V)	SDIO Reset# (O)(0.1.8V)	27
26	UART Wake# (I/O)(0.3.3V)	SDIO Wake# (I/O)(0.1.8V)	25
24	SDIO DAT3 (I/O)(0.1.8V)	SDIO DAT3 (I/O)(0.1.8V)	23
22	SDIO DAT2 (I/O)(0.1.8V)	SDIO DAT2 (I/O)(0.1.8V)	21
20	SDIO DAT1 (I/O)(0.1.8V)	SDIO DAT1 (I/O)(0.1.8V)	19
18	GND	SDIO DAT0 (I/O)(0.1.8V)	17
16	LED#2 (I/O)(0.1.8V)	SDIO DAT0 (I/O)(0.1.8V)	15
14	PCM_OUT/IS_SD_OUT (O)(0.1.8V)	SDIO DAT0 (I/O)(0.1.8V)	13
12	PCM_IN/IS_SD_IN (I/O)(0.1.8V)	SDIO CMD (I/O)(0.1.8V)	11
10	PCM_SYNC/IS_WS (O)(0.1.8V)	SDIO CMD (I/O)(0.1.8V)	9
8	PCM_CLK/IS_SCK (O)(0.1.8V)	SDIO CLK (O)(0.1.8V)	7
6	LED#1 (I/O)(0.1.8V)	GND	5
4	3.3V	USB_D-	3
2	3.3V	USB_D+	1

(link to PICE Port 6)
PCIE X1

(From PCH CLKOUT1)
PCIE CLK



KEY E



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				0.1	
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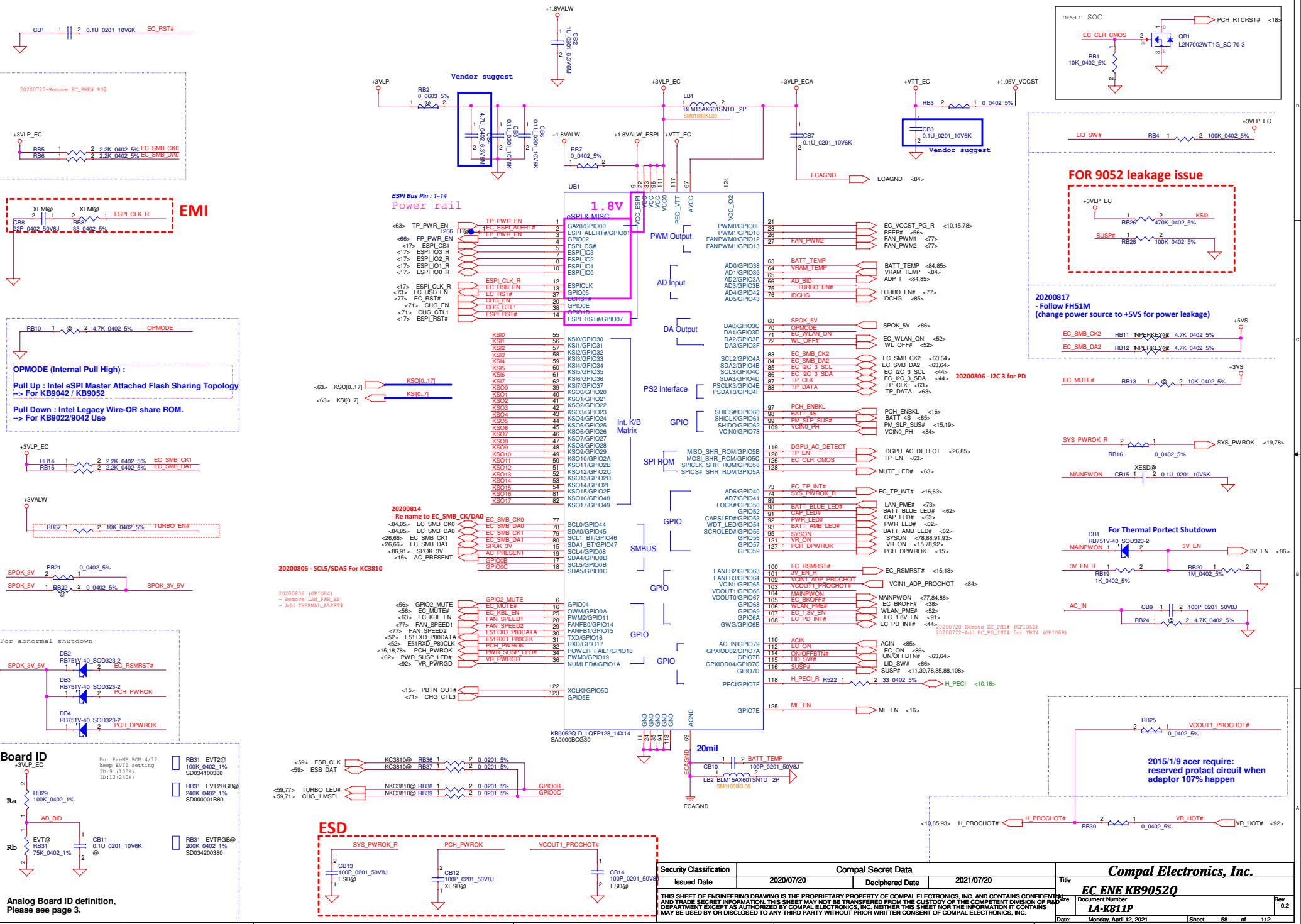
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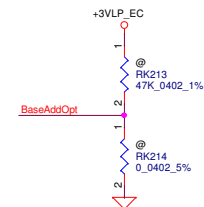
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*NMI_DBG#: is a debug pin for EC to inform BIOS after press hot key.



[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and
the other keep NC or initial High

- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08



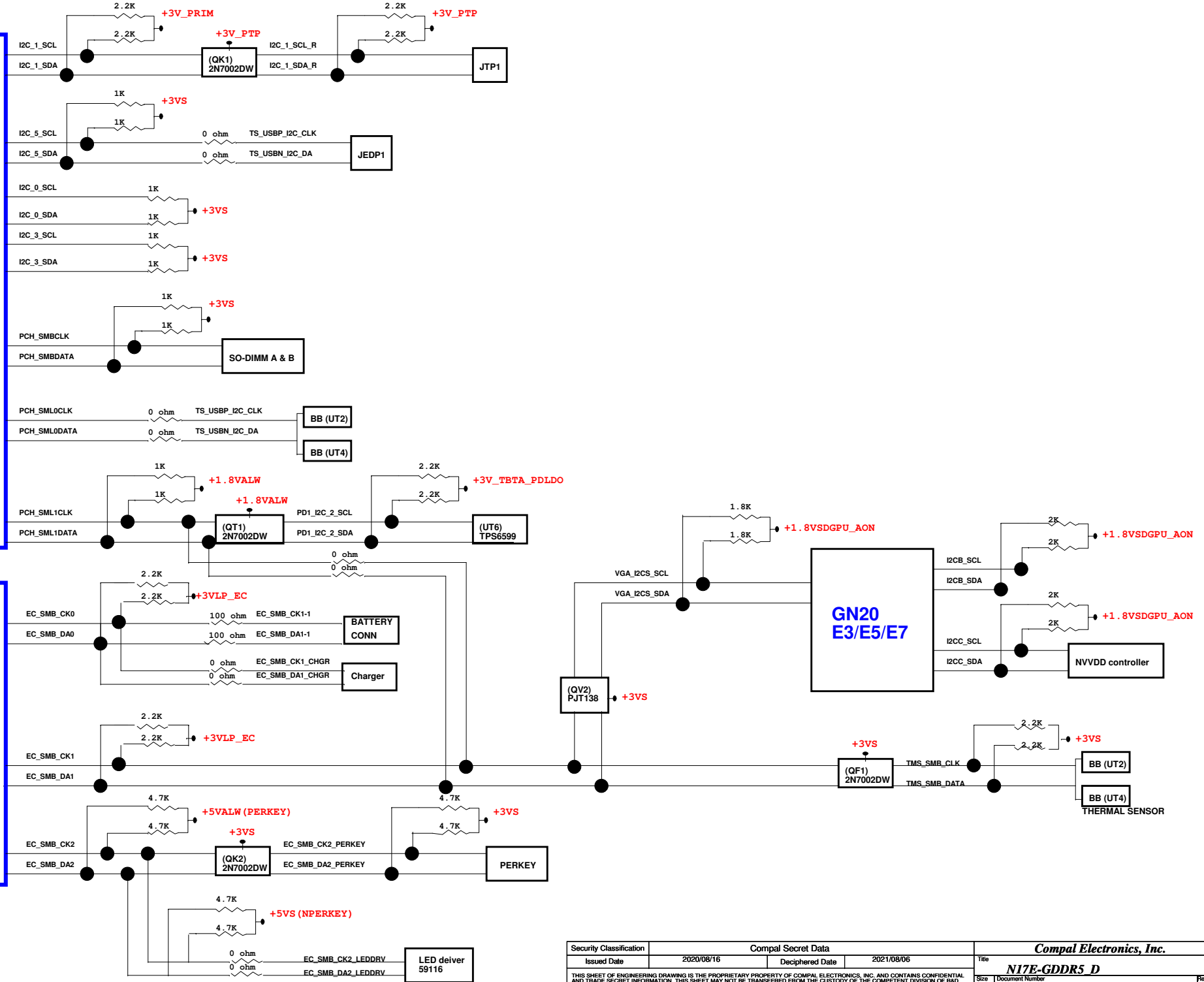
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								Size		Document Number		Rev	
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								Date: Monday, April 12, 2021		Sheet 59 of 112			

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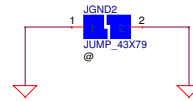
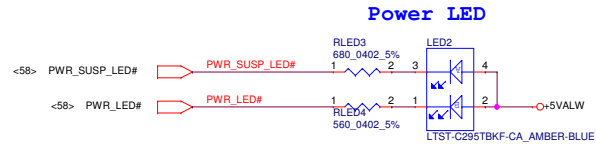
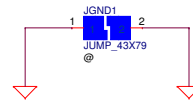
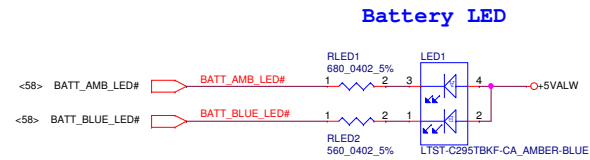
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				0.1	
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Tiger lake
PCH - H

KB9052

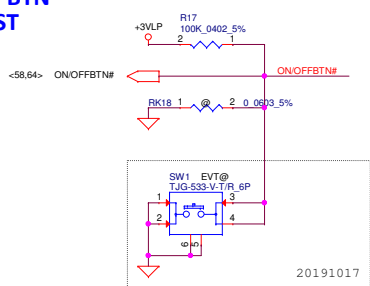


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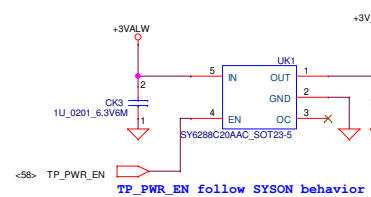


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Issued Date	2020/08/16	Deciphered Date	2021/08/06	Title	LED	
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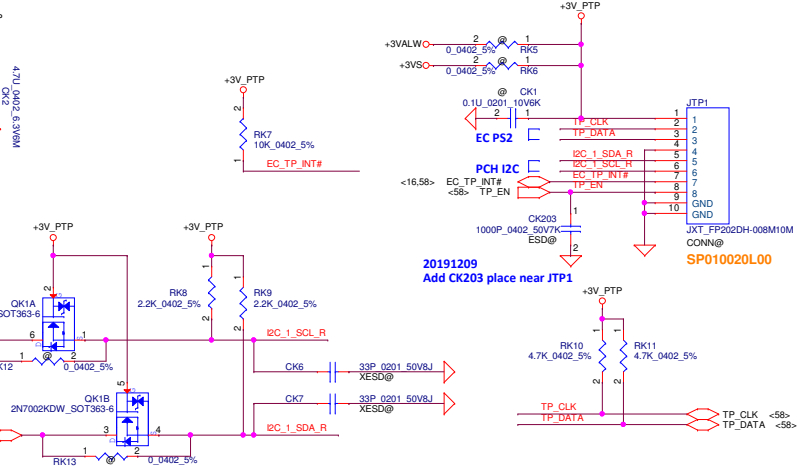
ON/OFF BTN
- For TEST



Touch Pad



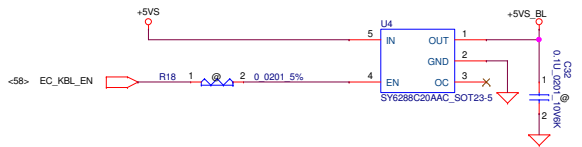
remove ESD symbol for layout reason



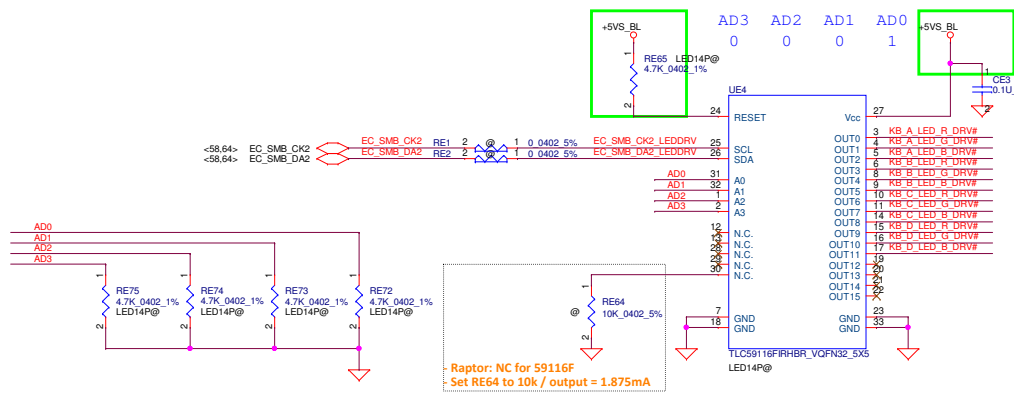
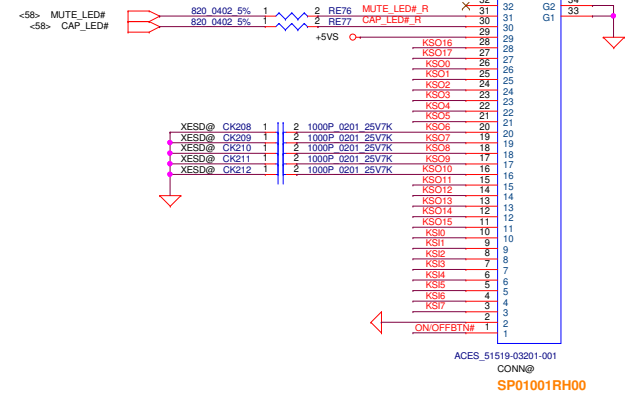
LED driver

20191016
- Remove QE62/RE70/RE69
- PU +5VALW @ EC

20191001
- Change to +5VS only
- KBL_EN only (Check EC Code)
- pop (Normal & RGB)

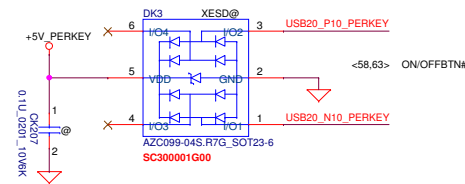
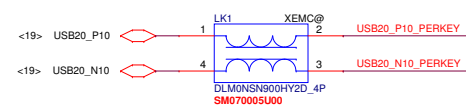
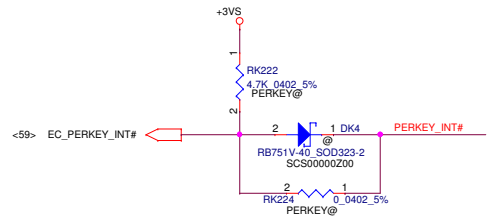
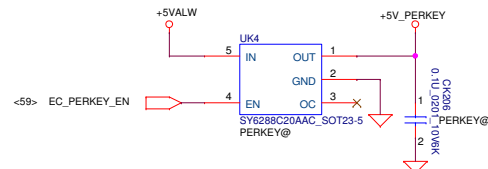
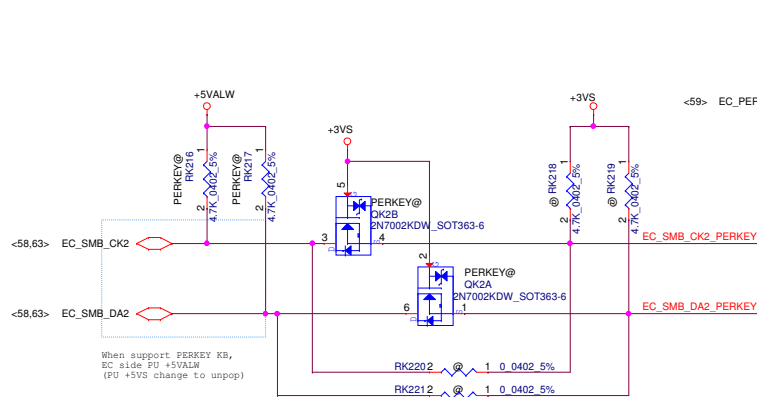


KB Conn. / Backlight

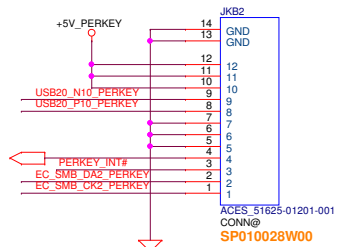


Raptor: NC for 59116F
- Set RE64 to 10K / output = 1.875mA

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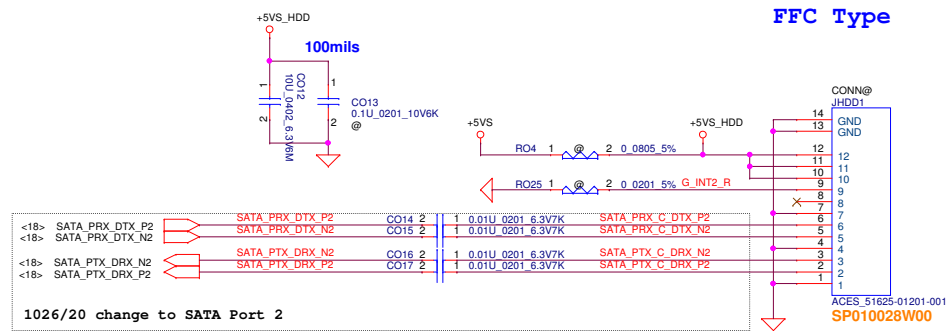
Per Key Conn.



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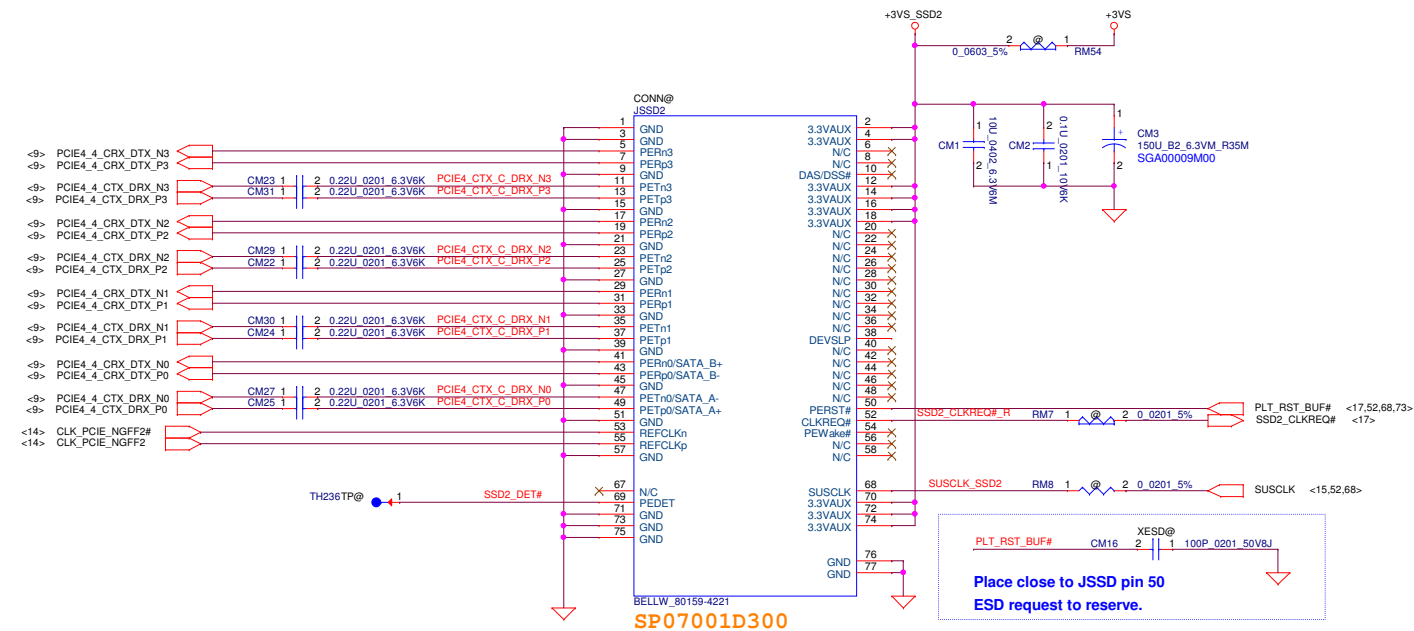
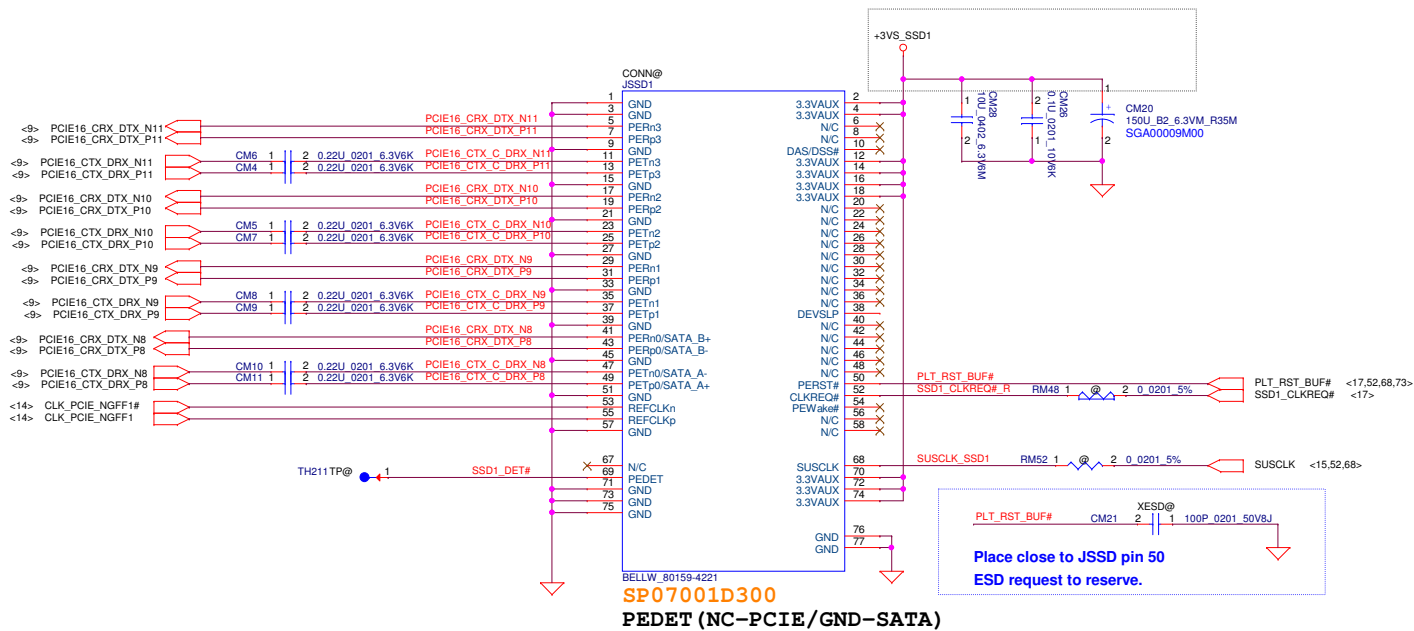
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20190918

Remove HDD Re-driver

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								Size	Document Number	Rev
								Custom	GH51M MB LA-J862P	0.1
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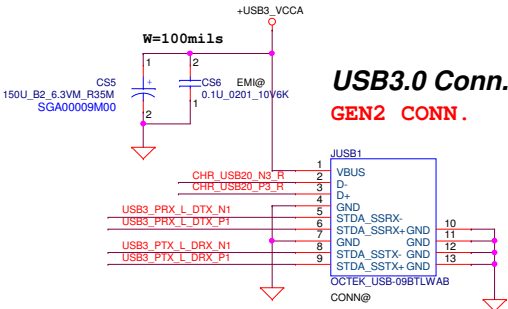
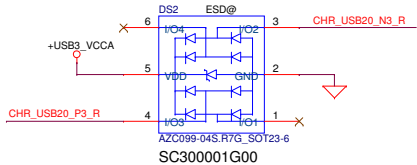
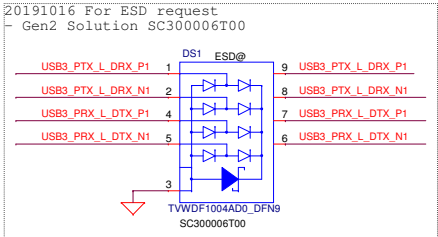
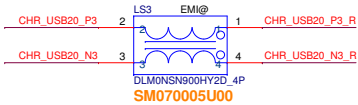
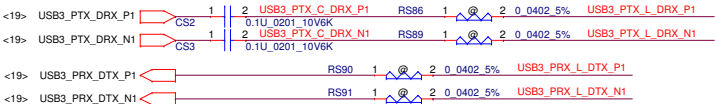
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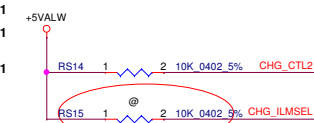
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USB3.0



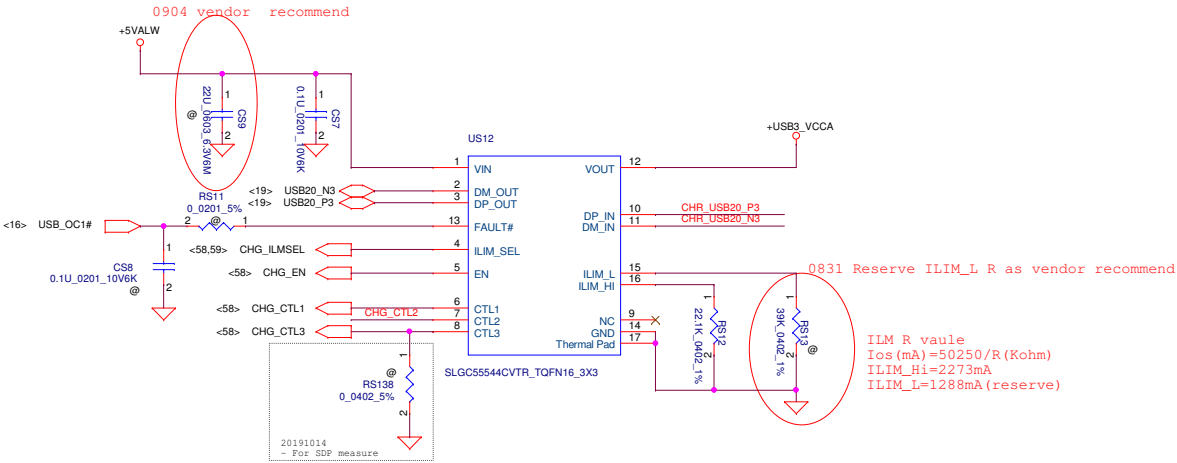
USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	1	0	1		SDP1-OFF	ILIM_H	Port power off
0	1	0	1		SDP1	ILIM_H	Data Lines Connected
0	1	1	1		DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1		CDP	ILIM_H	Data Lines Connected

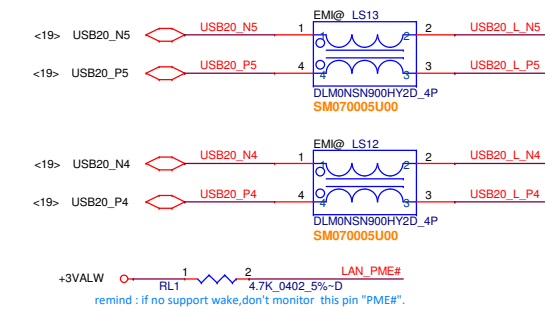


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20190918
USB3 Port3 move to IO/B

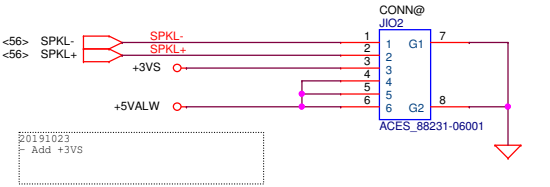
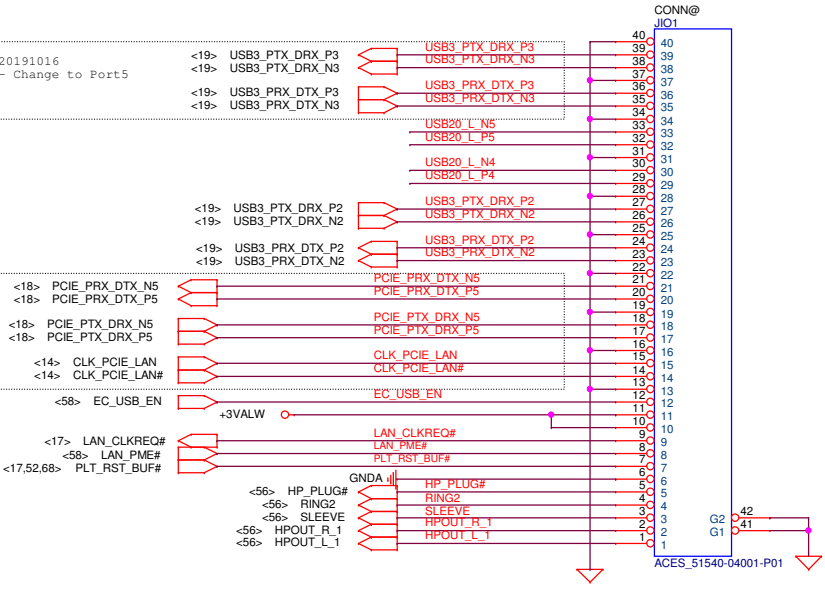
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IO/B CONN



20191016
- Change to Port5

20191008
- LAN PCIe&CLK Remove AC Cap > Vender confirm
(CL136/137/138/139)



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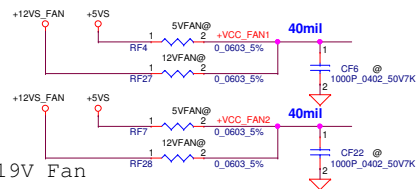
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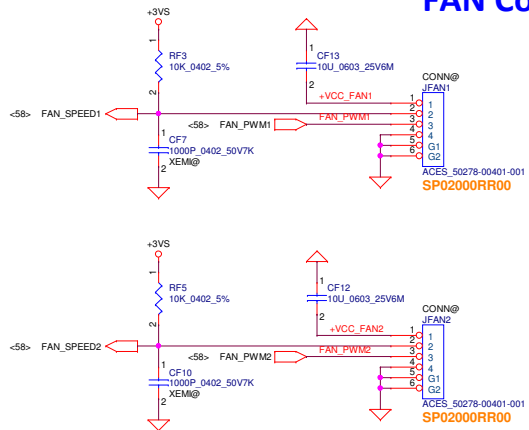
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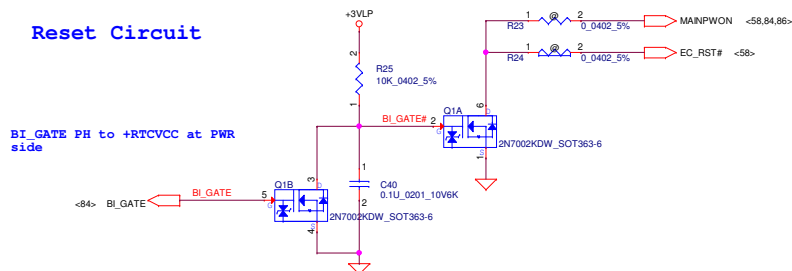
20200914
- Remove 19V Fan



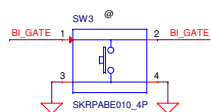
FAN Conn



Reset Circuit

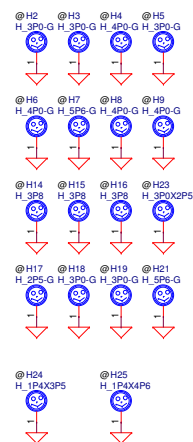


Reset Button



change PN to SN10000CV00

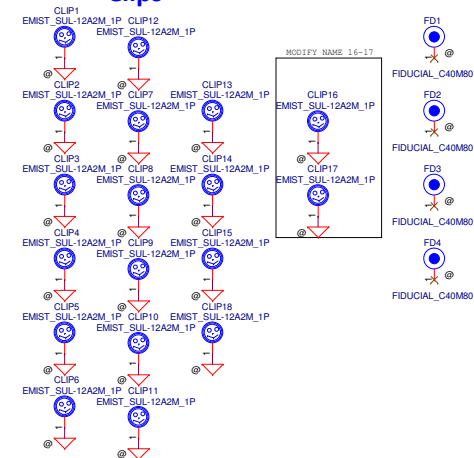
Screw Hole



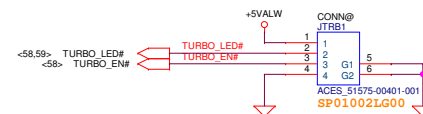
Stand OFF



Clips

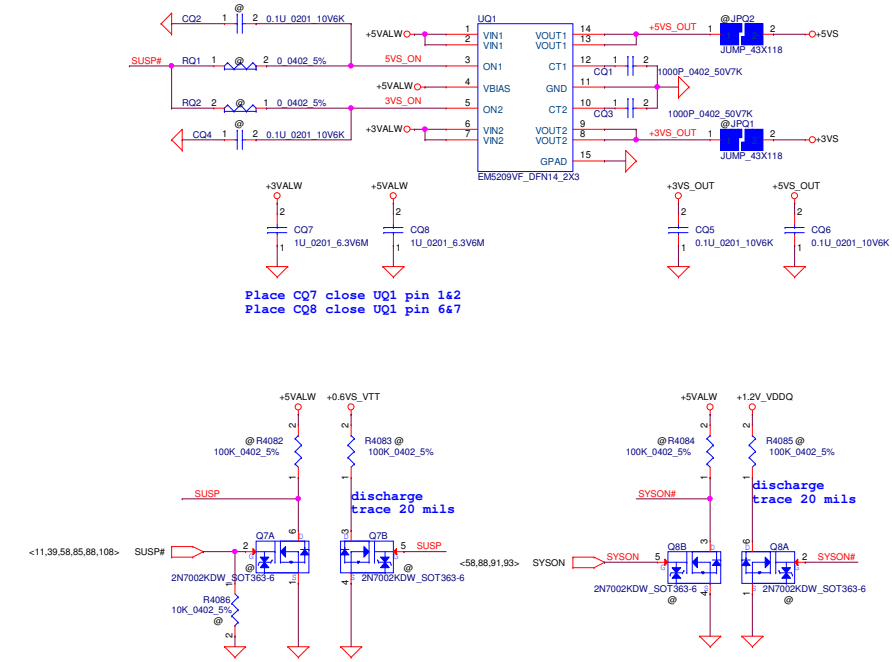


Turbo Key

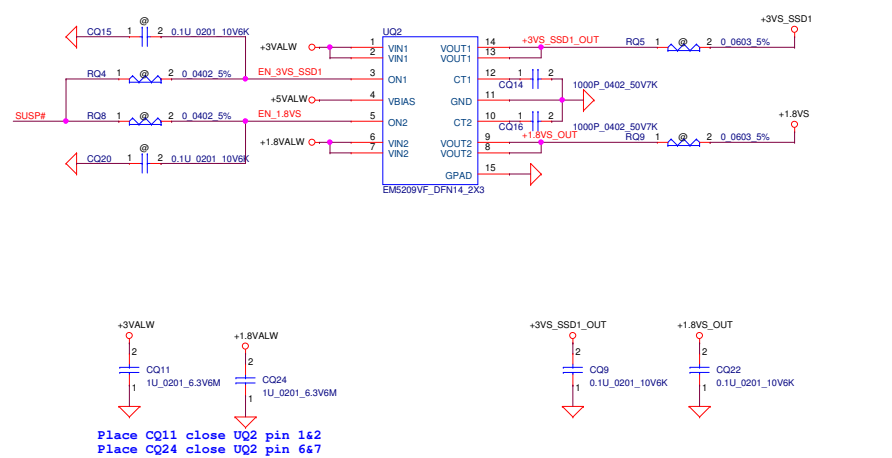


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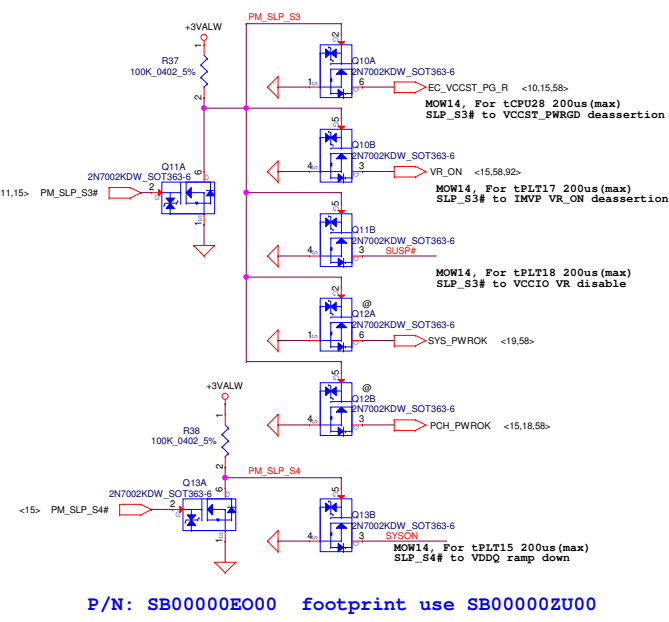
System DC interface



+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



For Power ON/Off Sequence



+1.05VALW out put from PCH

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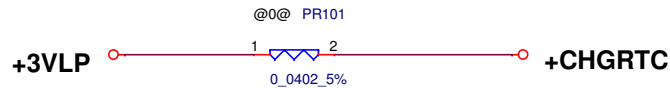
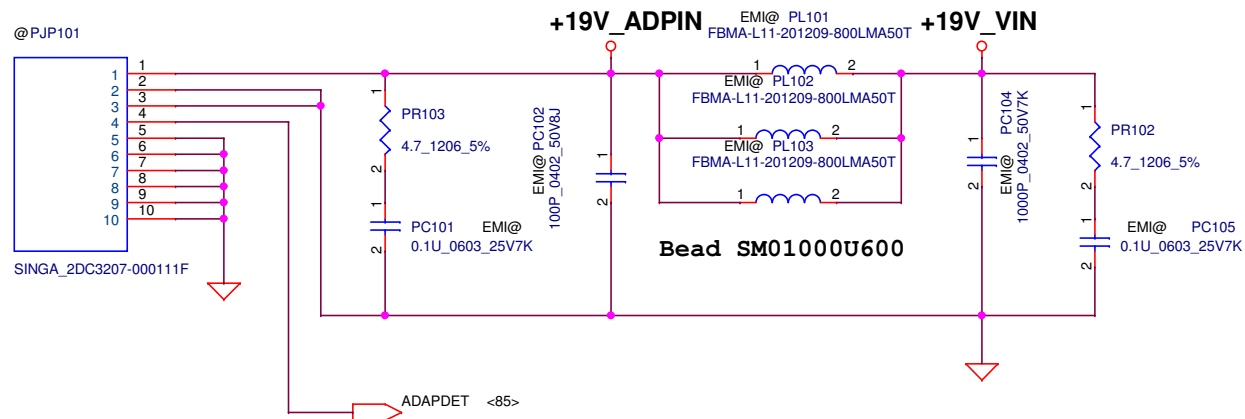
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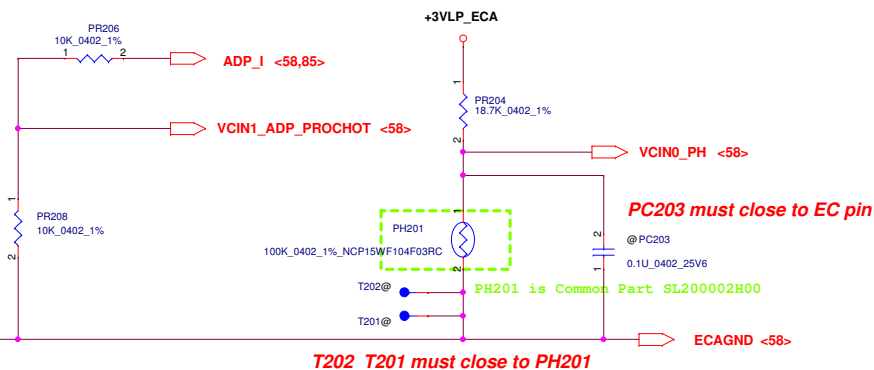
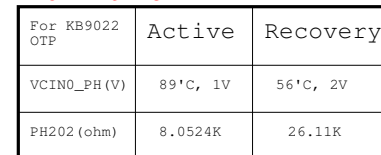
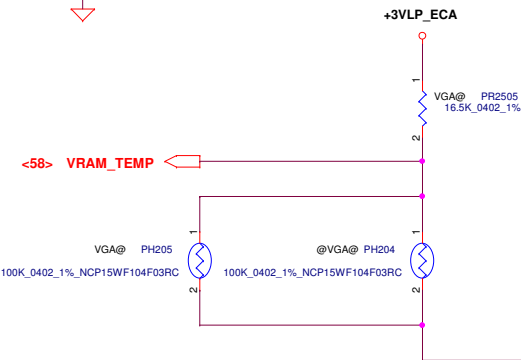


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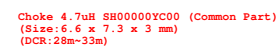
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PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



```
ADP_I=20*I(adapter)*0.01
I(adapter)=adapter(W)*130%/19
```

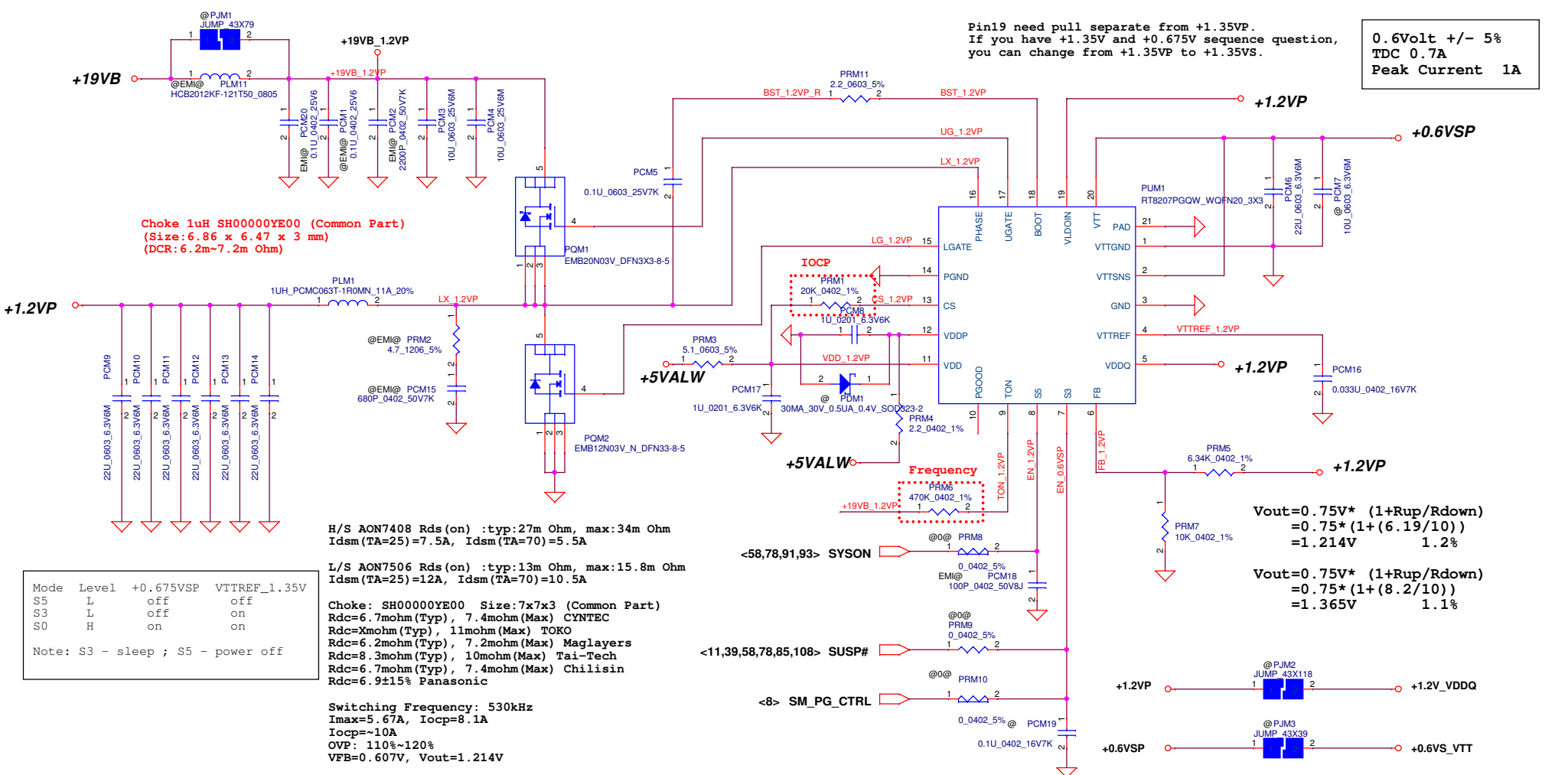
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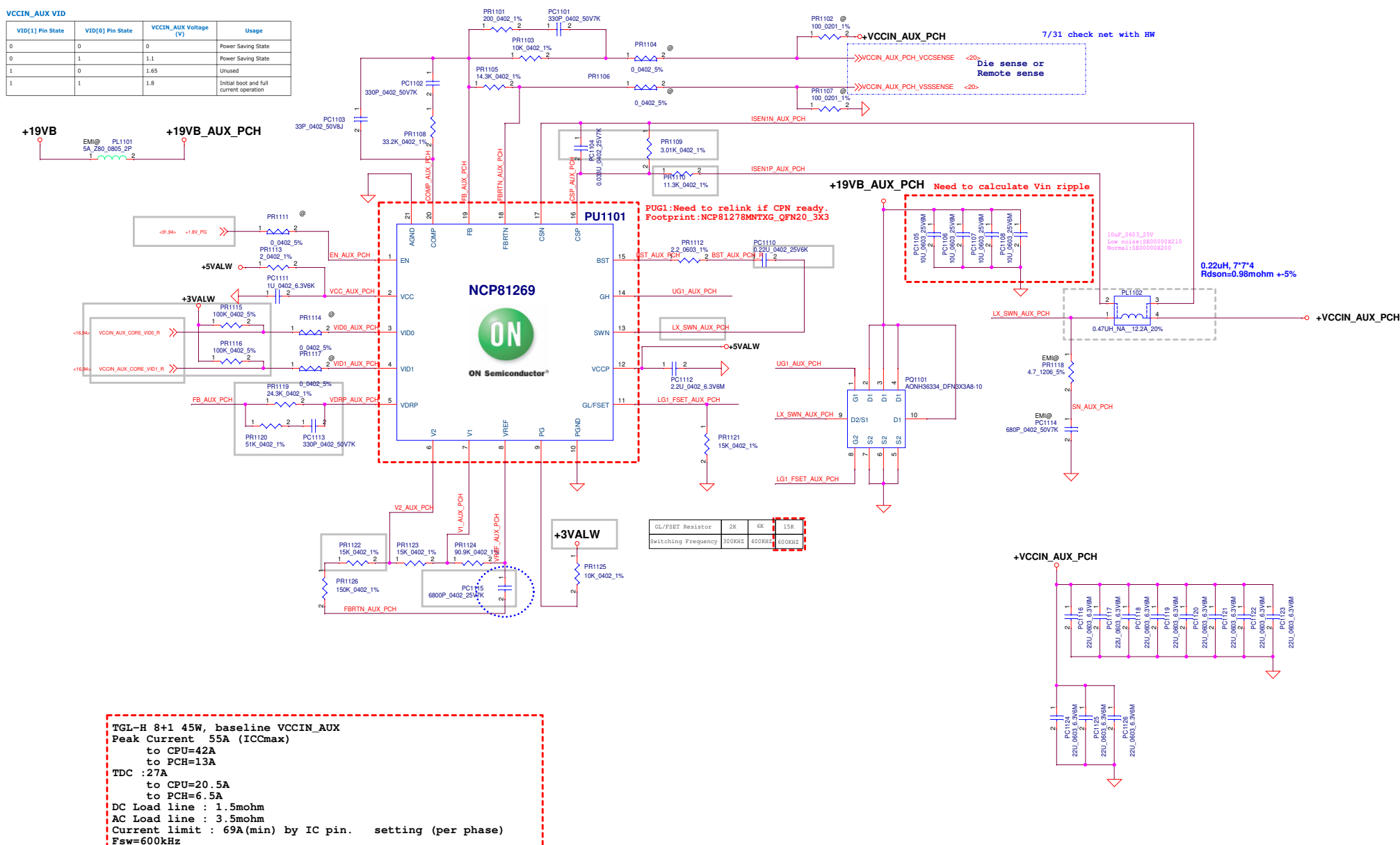
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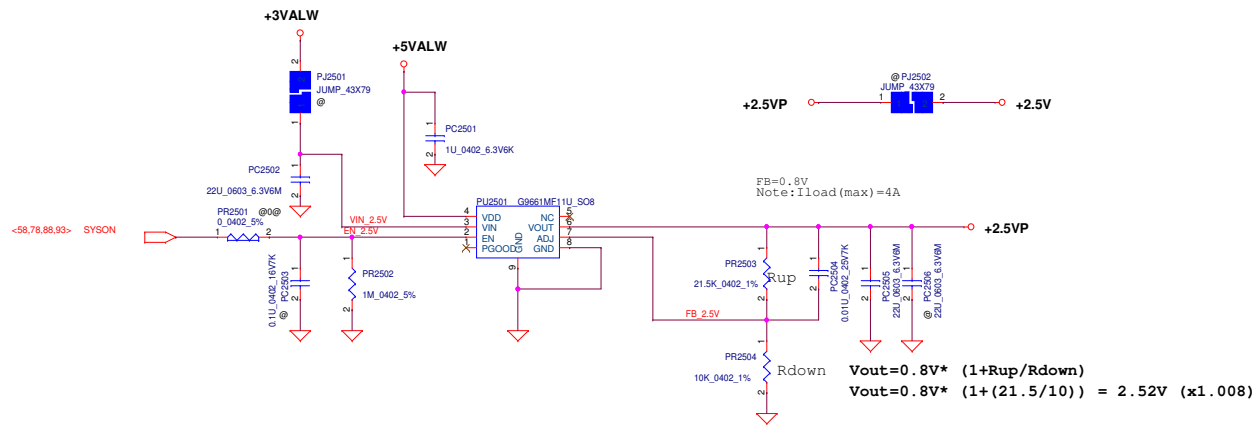
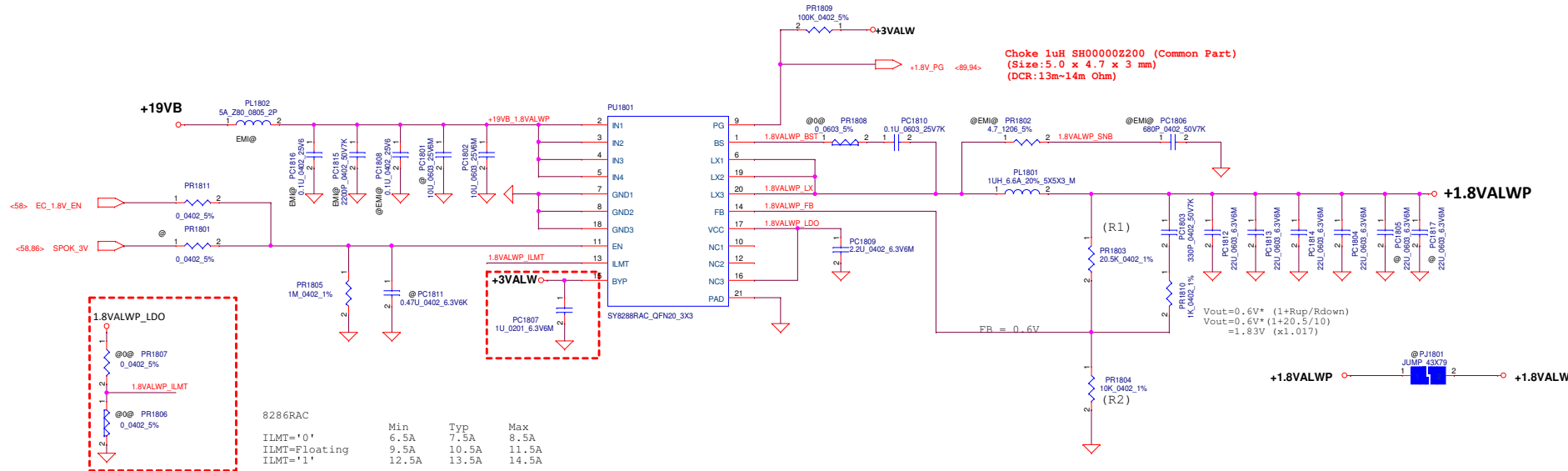
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0	0	0	Power Saving State
0	1	1.1	Power Saving State
1	0	1.65	Unused
1	1	1.8	Initial boot and full current operation



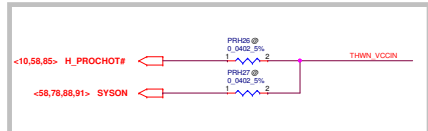
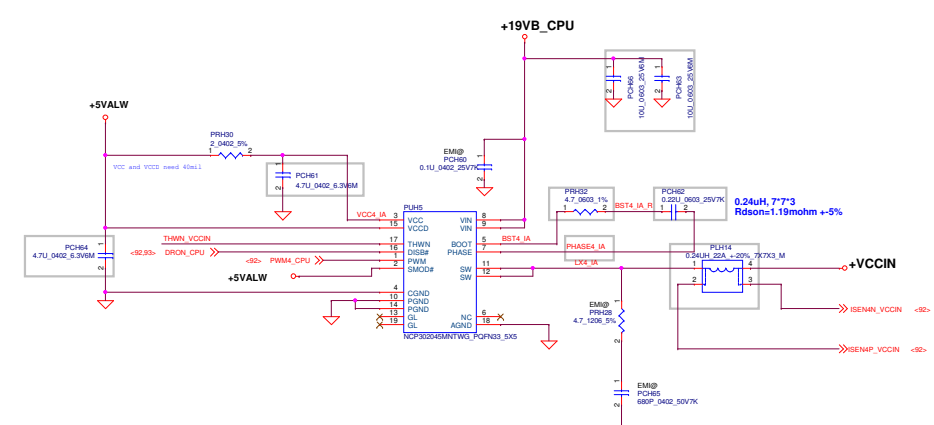
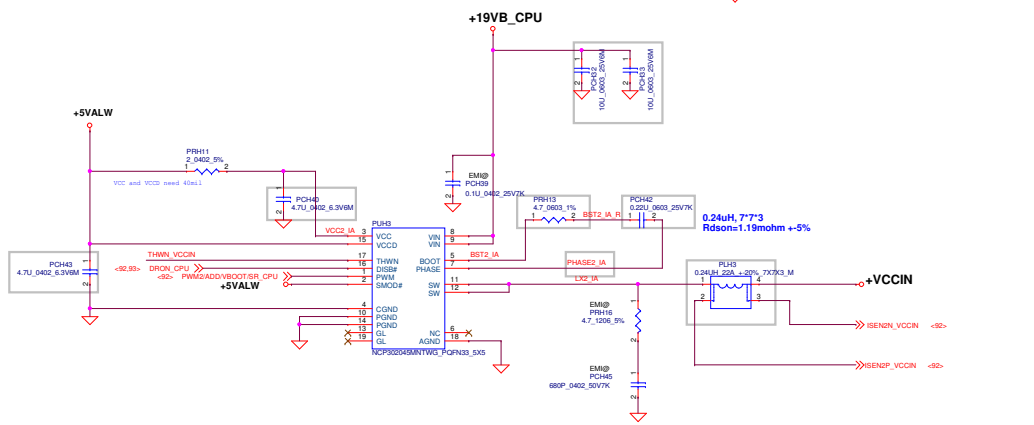
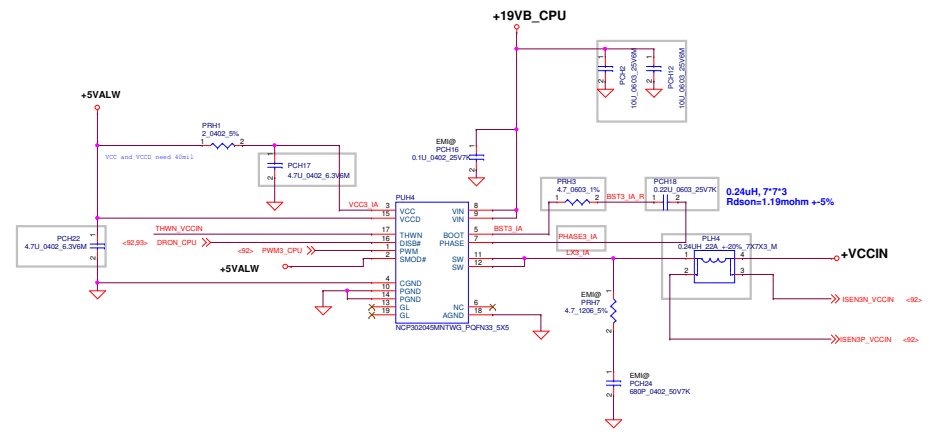
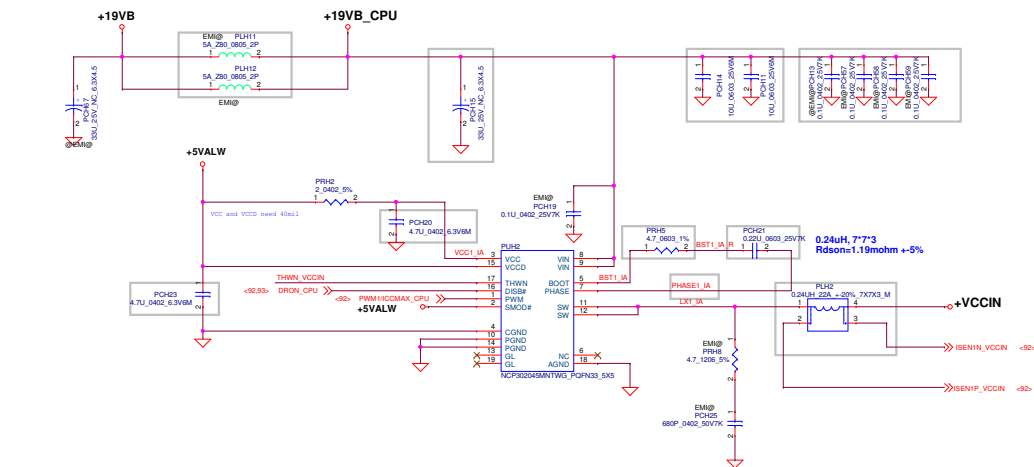
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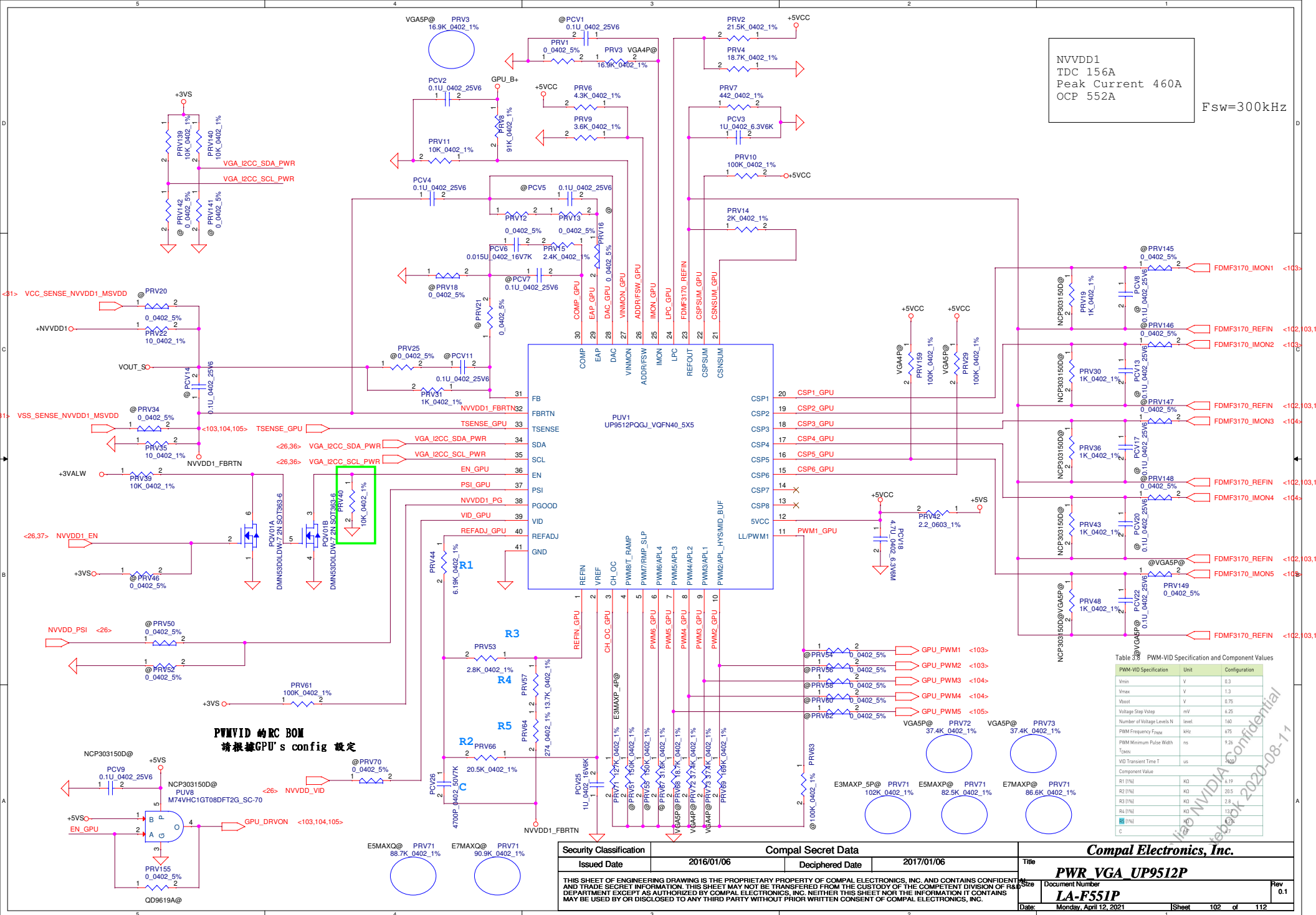
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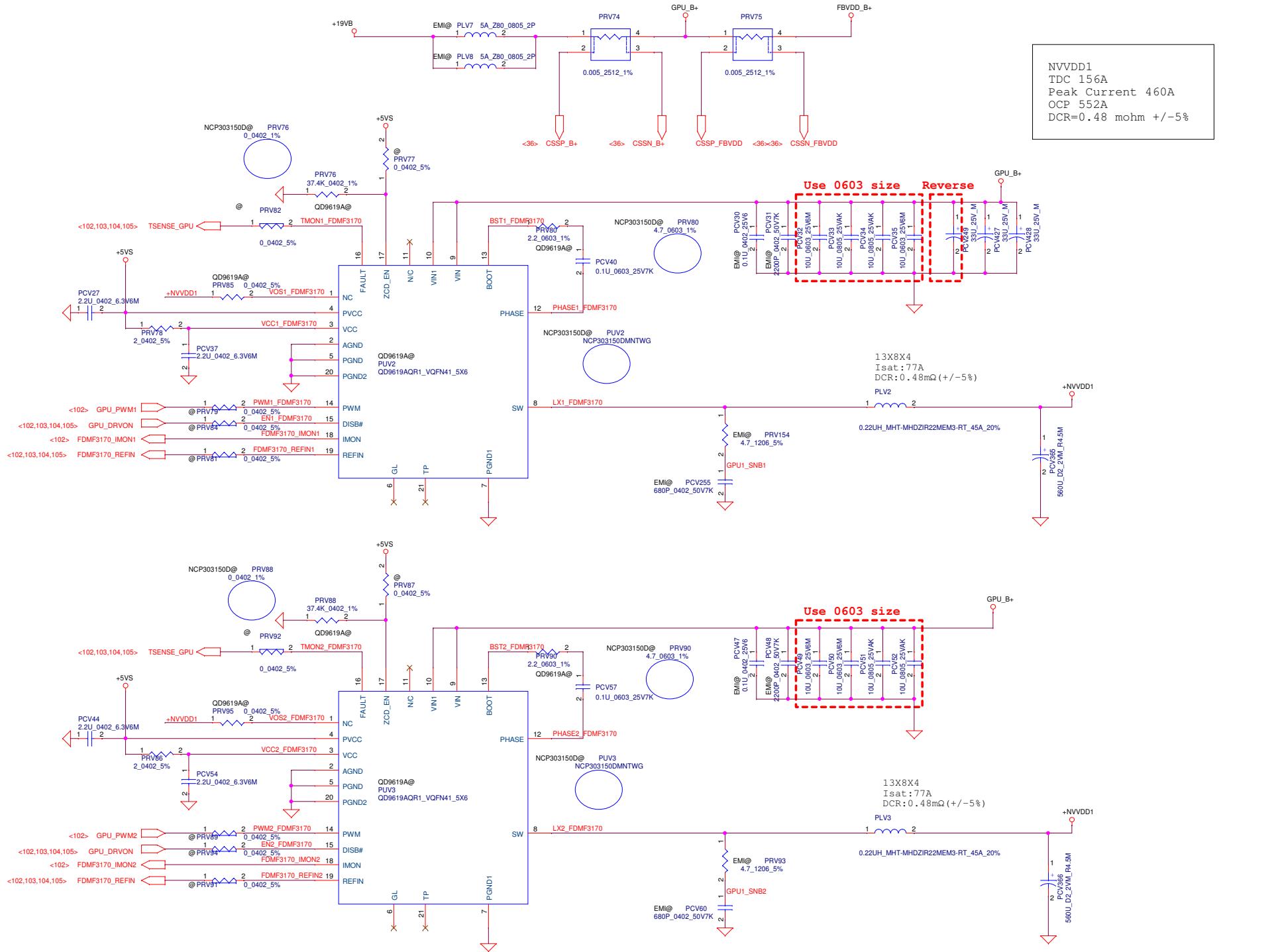
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PWMVID 的 RCON
请根据GPU's config 设定

Table 3. PWM-VID Specification and Component Values

PWM-VID Specification	Unit	Configuration
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.75
Voltage Step Voltage	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency Fpwm	kHz	675
PWM Minimum Pulse Width	ns	9.26
Tonset	ns	120
VID Transient Time T	us	100
Component Value		
R1 (1N)	KΩ	5.19
R2 (1N)	KΩ	20.5
R3 (1N)	KΩ	2.8
R4 (1N)	KΩ	12
R5 (1N)	KΩ	12



NVVDD1
TDC 156A
Peak Current 460A
OCP 552A
DCR=0.48 mohm +/-5%

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